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MS-7996

ATX:235*180

Ver: 14

Intel -SkyLake-S plamform

CPU:

LGA1151
CPU POWER PAK *3 Phase
GT POWER PAK *2 Phase

System Chipset:

SPT-H :B150
SPT-H :H150

Onboard Chip:

HD Audio Codec: ALC892
SIO: NCT5565D
Flash ROM: SPI 64 MB
DP to VGA: ITE6515

PWM:

VCORE - RT3606
DDR - RT8231
PCH(1.0V) - UP1540
VCCSA - RT8125C
VCCIO - NB681(Converter)
VPP25 - MP2147

Main Memory:

DDR4 * 2 (Dual Channel)

LDO:

VCCSTPLL - GS7133

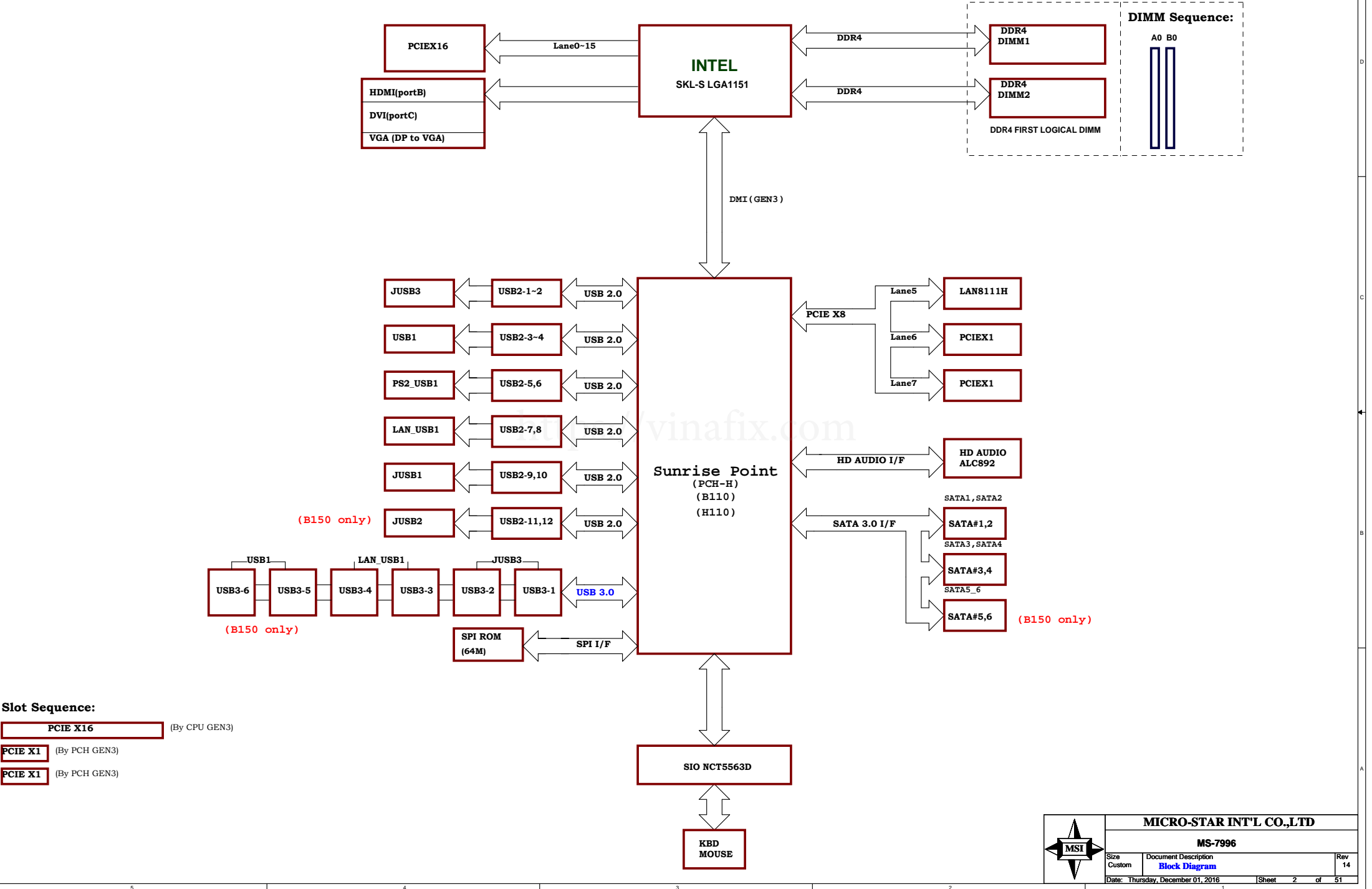
ACPI:

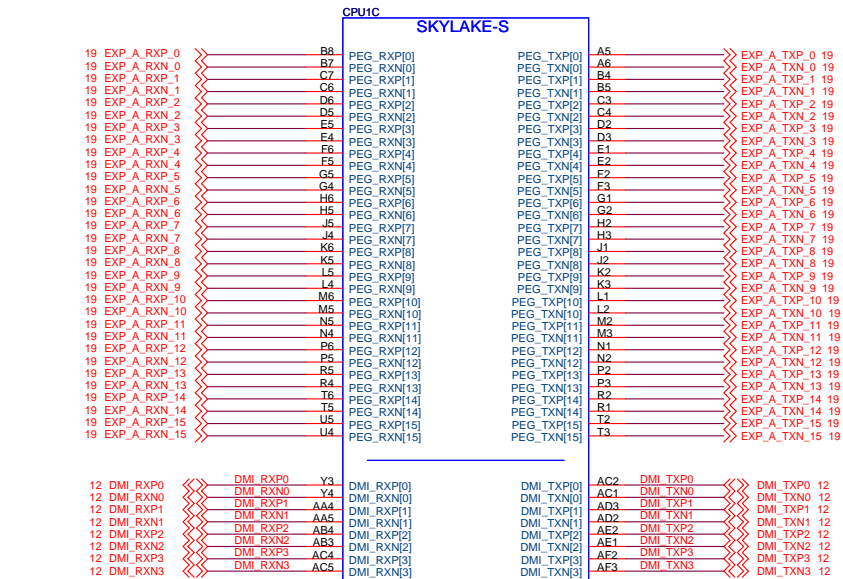
5VDAUL:uP7501
5VDIMM:uP7501
3VSB:GS7133+PN MOS
3VDSW:GS7133

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2

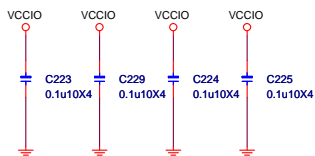
MS-7996 Block Diagram





VCCIO R2 24.9R1%4 PEG_COMP L7 PEG_RCOMP

L<=0.4 inch

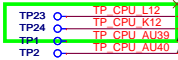


For DMI reference VCCIO USE
please close to DMI via side

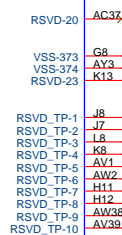
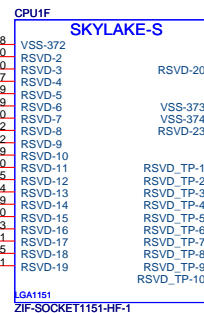
CRB 1.0 update
Add TP23,TP24
For Test

CRB 1.0 update
TP25
For Test

2014.09.24



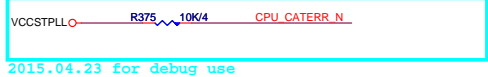
2014.09.24



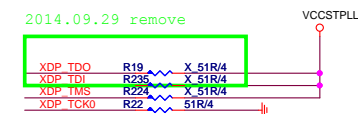
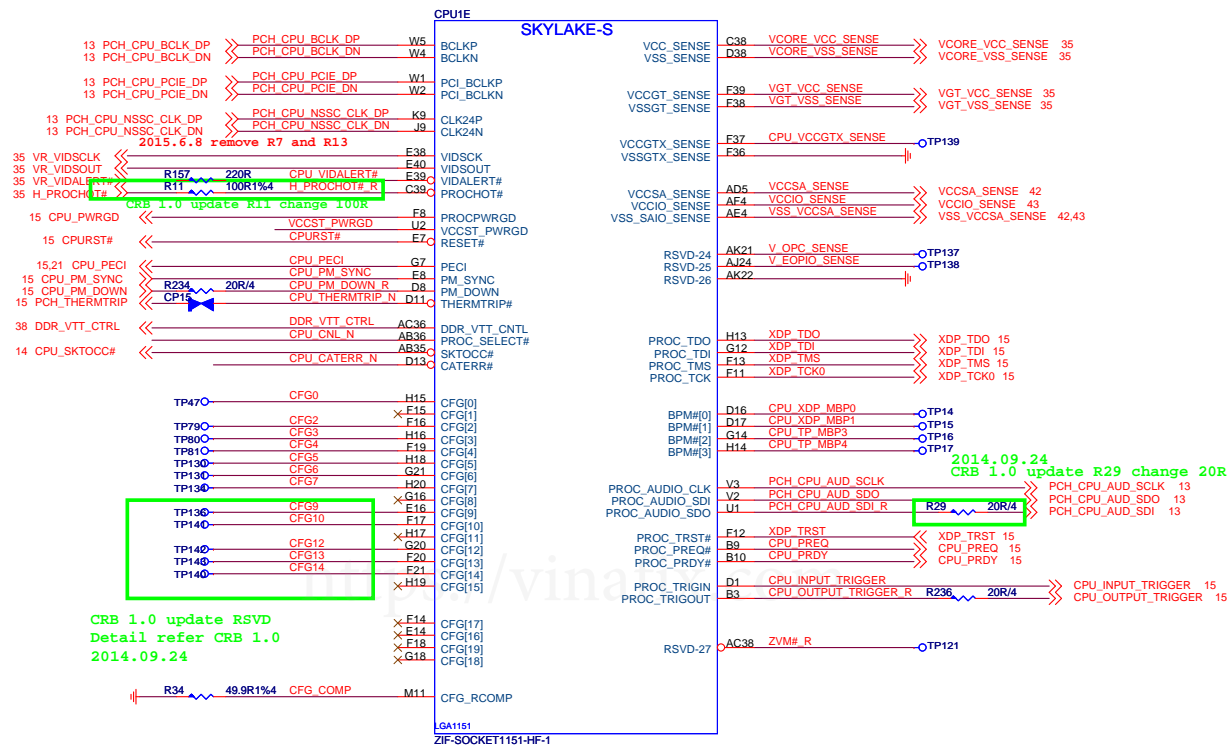
2014.09.24

CRB 1.0 update
CRB unstuff
PCB come back remove

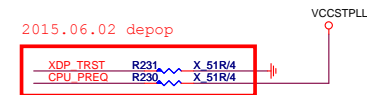
Vinafix.com



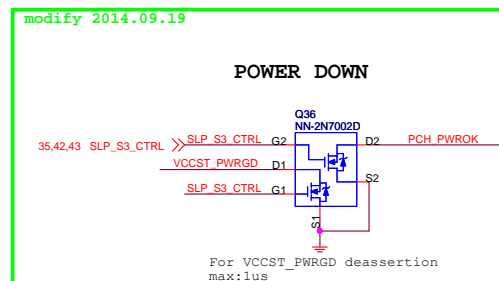
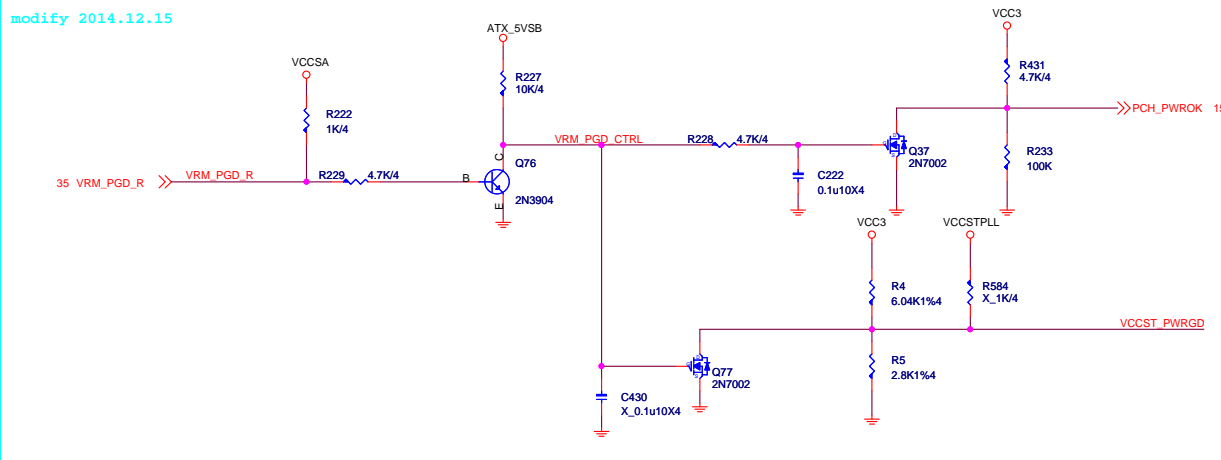
CFG Strap



Close CPU <1100 mil
1000 mil < CPU XDP MBP0~1 < 6000 mil



2015.06.02 depop



For VCCST_PWRGD deassertion
max:lus

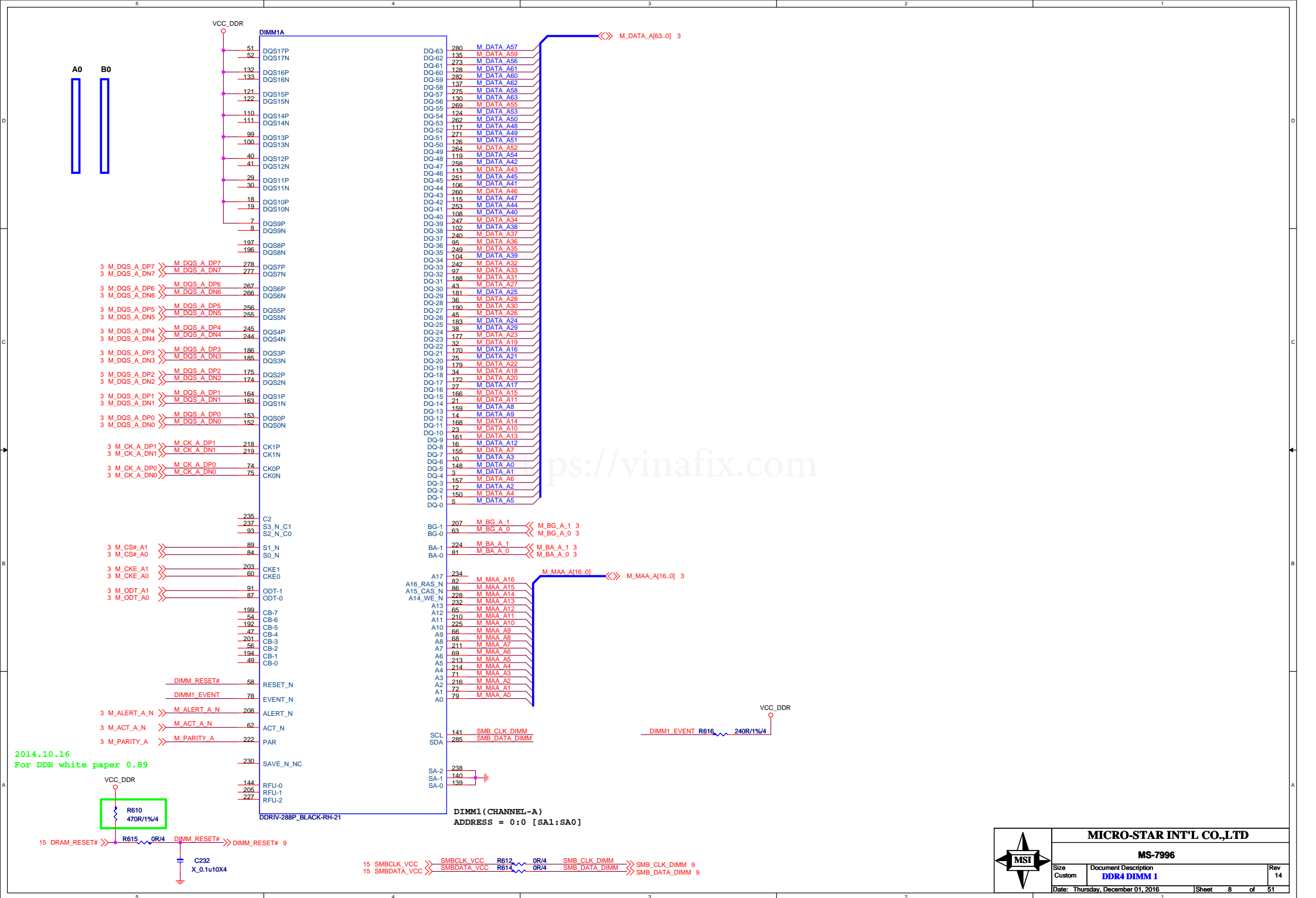


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Size Custom	Document Description CPU-Control/MISC/CFG/Audio	Rev 1
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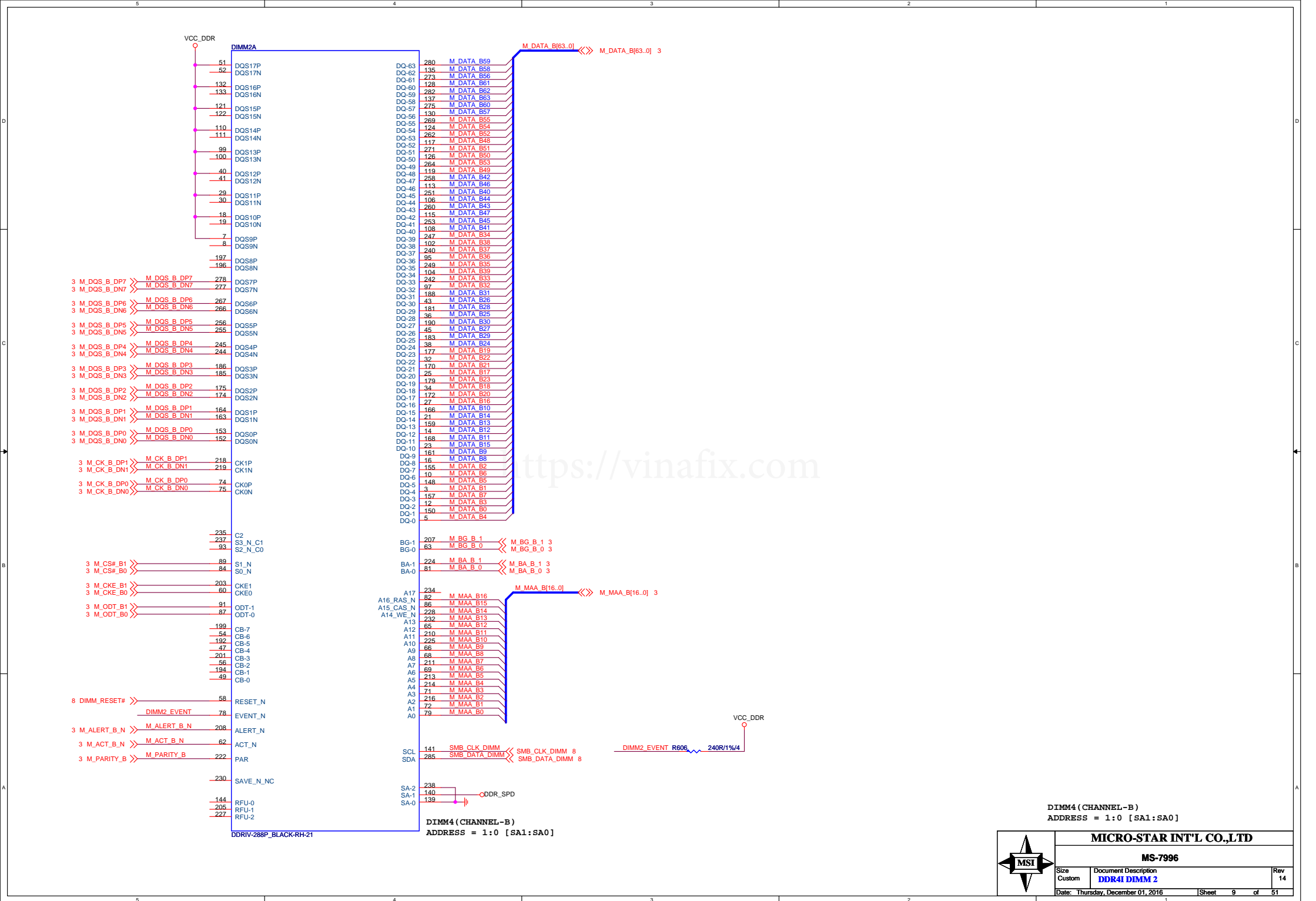
GND

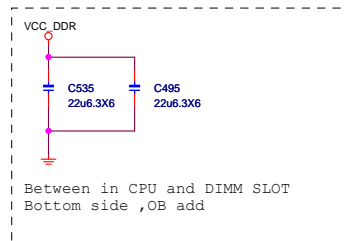
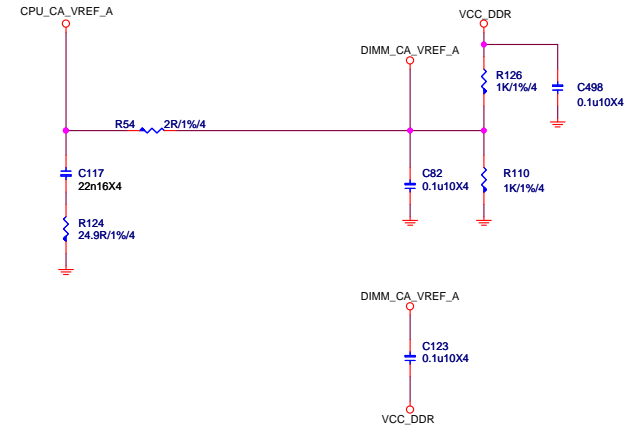
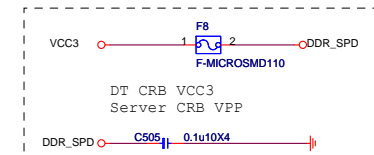
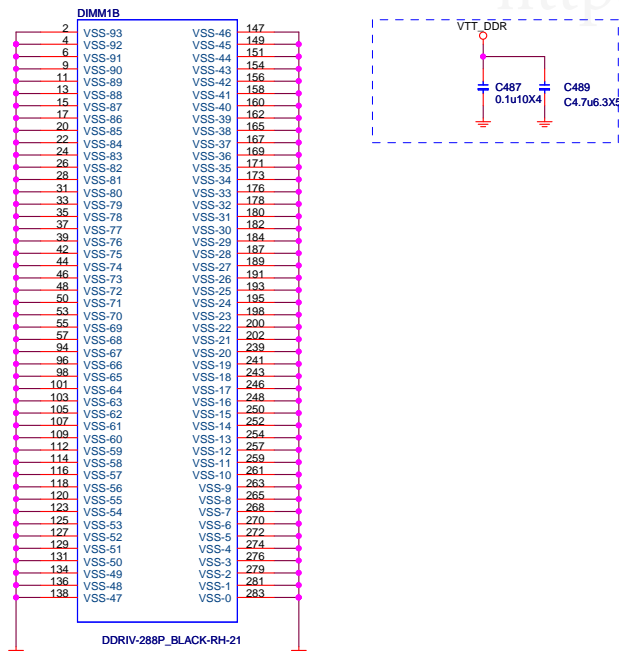
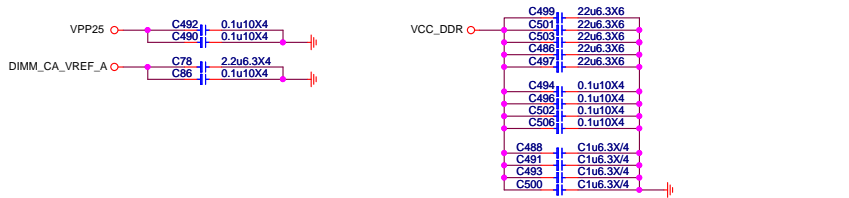
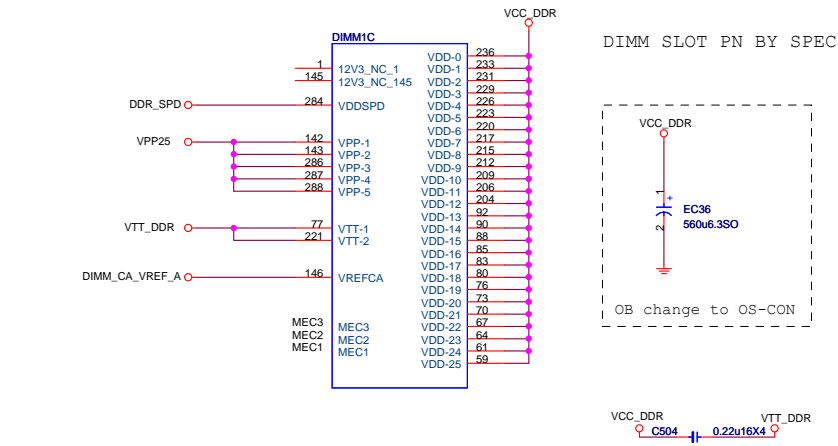


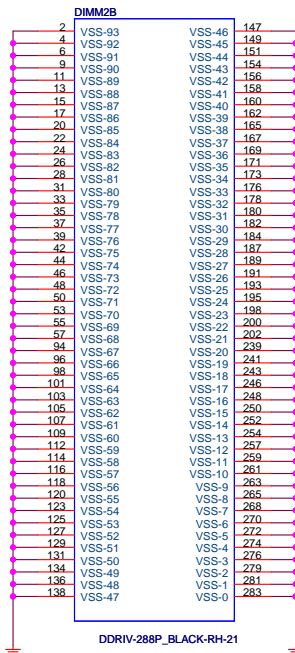
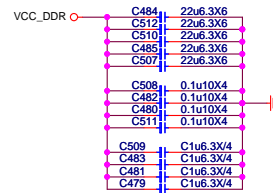
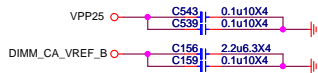
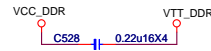
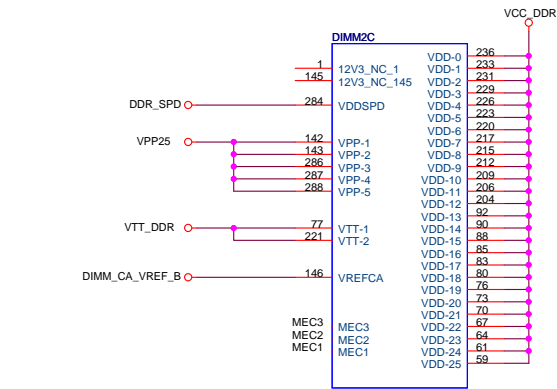
2014.10.16
For DDR white paper 0.89



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Custom	DDR4 DIMM 1	14
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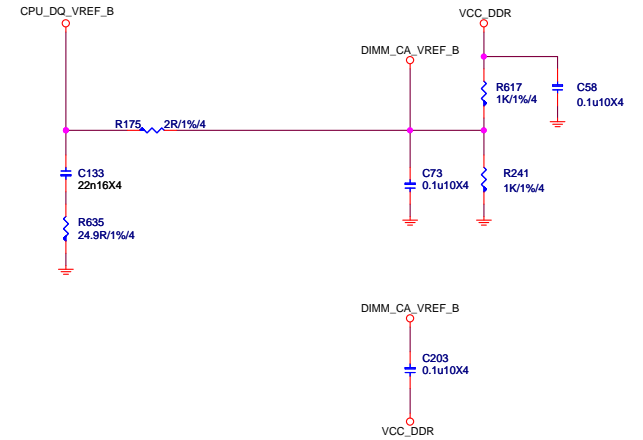
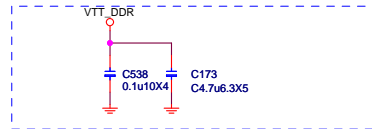


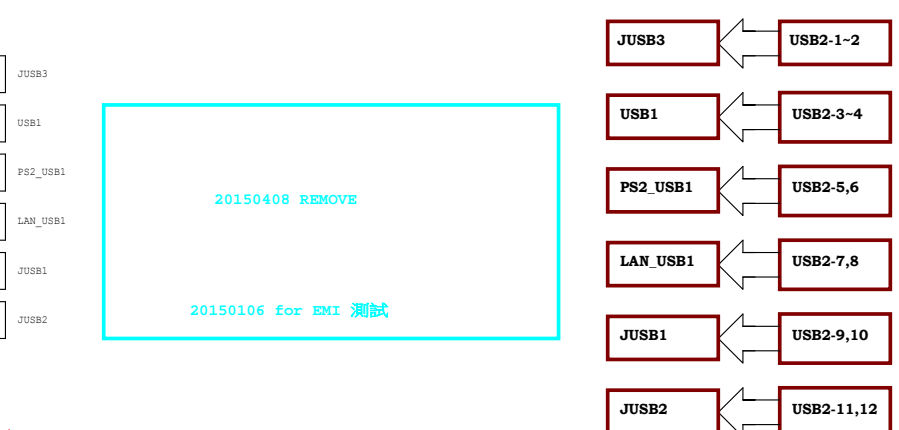
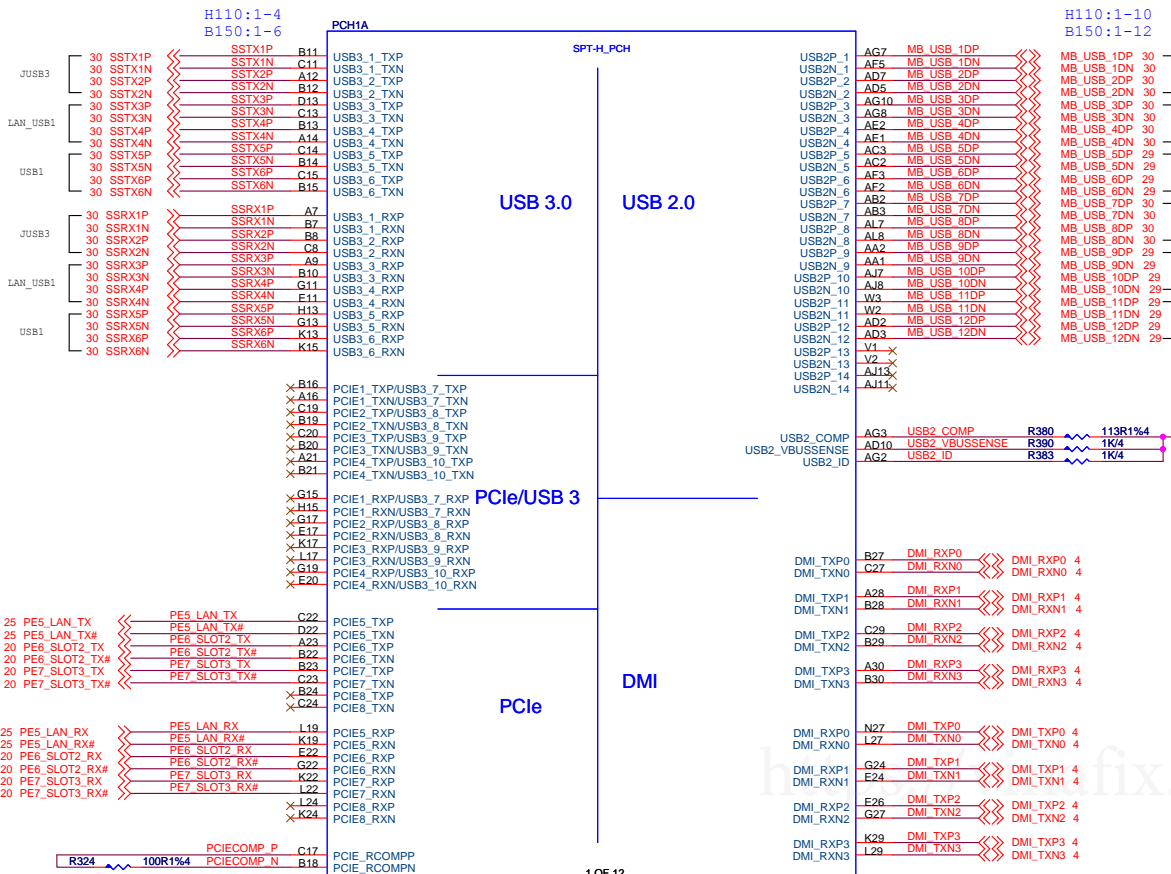




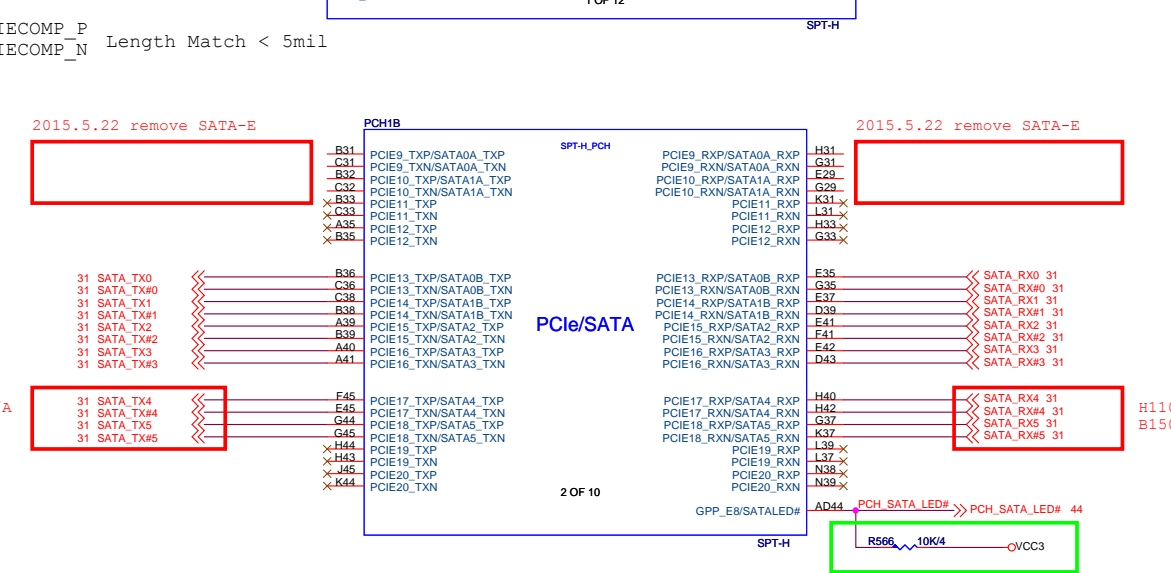
<https://vinafix.com>

0.1uFxl per dimm

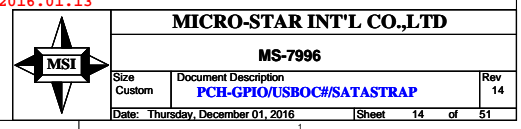


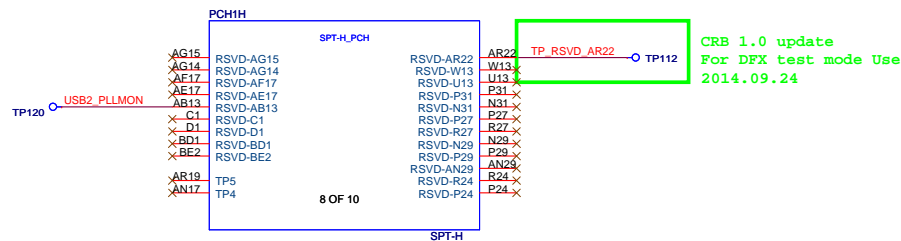
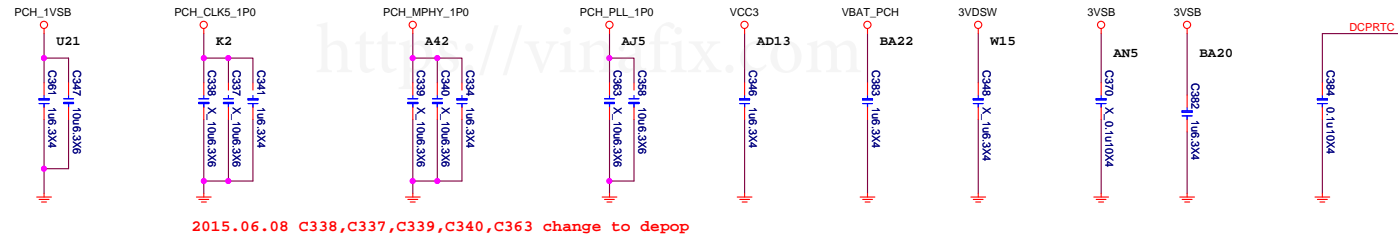


sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCle/LAN	PCle	PCle	PCle
B150	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCle/LAN	PCle	PCle	PCle
H170	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	USB3	USB3	PCle	PCle/LAN	PCle/LAN	PCle	PCle	PCle
Z170	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	USB3/PCle	USB3/PCle	USB3/PCle	PCle/LAN	PCle/LAN	PCle	PCle	PCle



Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCle/LAN	PCle	N/A	LAN	SATA*/LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
B150	PCle/LAN	PCle	N/A	LAN	SATA*/LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
H170	SATA	LAN	PCle	LAN	SATA	SATA	SATA	SATA	SATA	PCle	PCle	PCle	2
Z170	SATA	SATA	PCle	LAN	SATA	SATA	SATA	SATA	SATA	PCle	PCle	PCle	3





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GND

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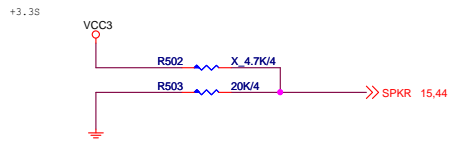


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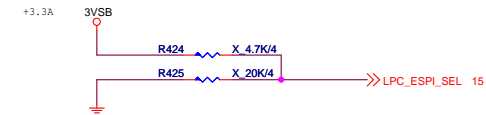
Size	Document Description	Rev
Custom	PCH-GND	14
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TOP Swap



Internal pull-down 20K is disabled after PLTRST#

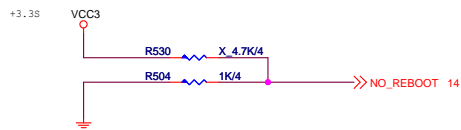
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

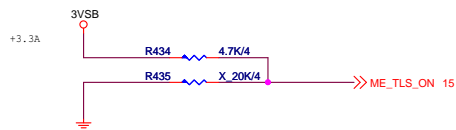
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

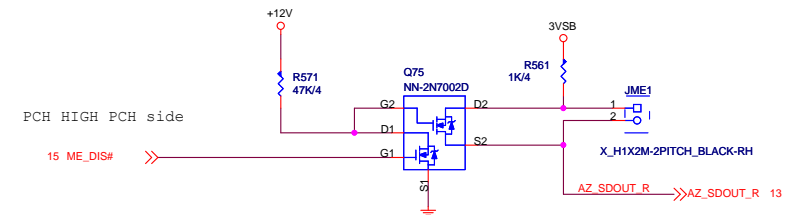
AMT and SBA with confidentiality



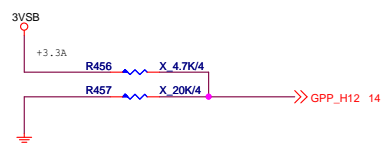
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

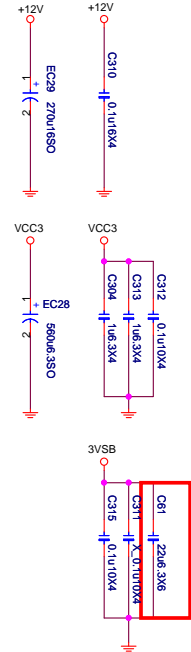
Internal pull-down 20K is disabled after RSMRST




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Custom	PCH-Strap teknisi indonesia	14
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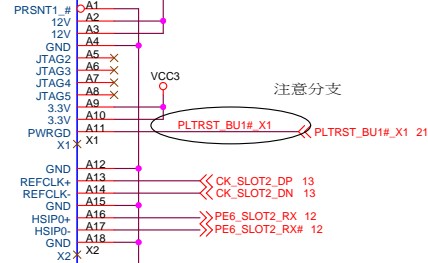
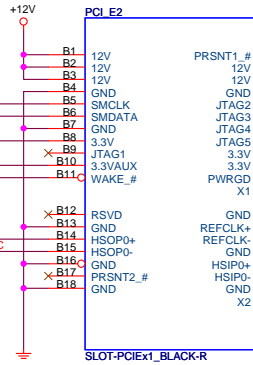
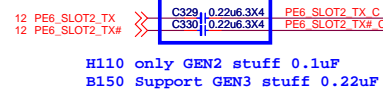


	MICRO-STAR INT'L CO.,LTD		
	MS-7996		
	Size Custom	Document Description PCIE SLOT-CPU(X16)	Rev 14
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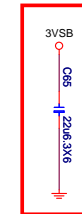
2015.6.8 change net_name to SMBCLK_VSB and SMBDATA_VSB



2014.12.29



2015.6.16 add C65

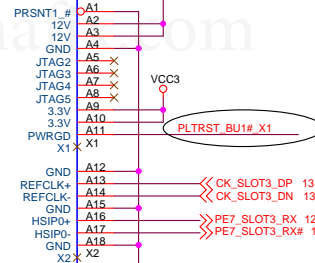
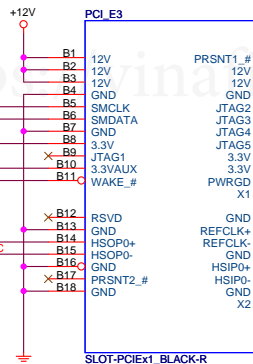
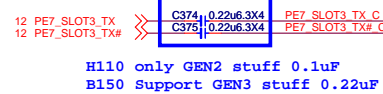


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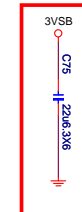
2015.6.8 change net_name to SMBCLK_VSB and SMBDATA_VSB



2014.12.29



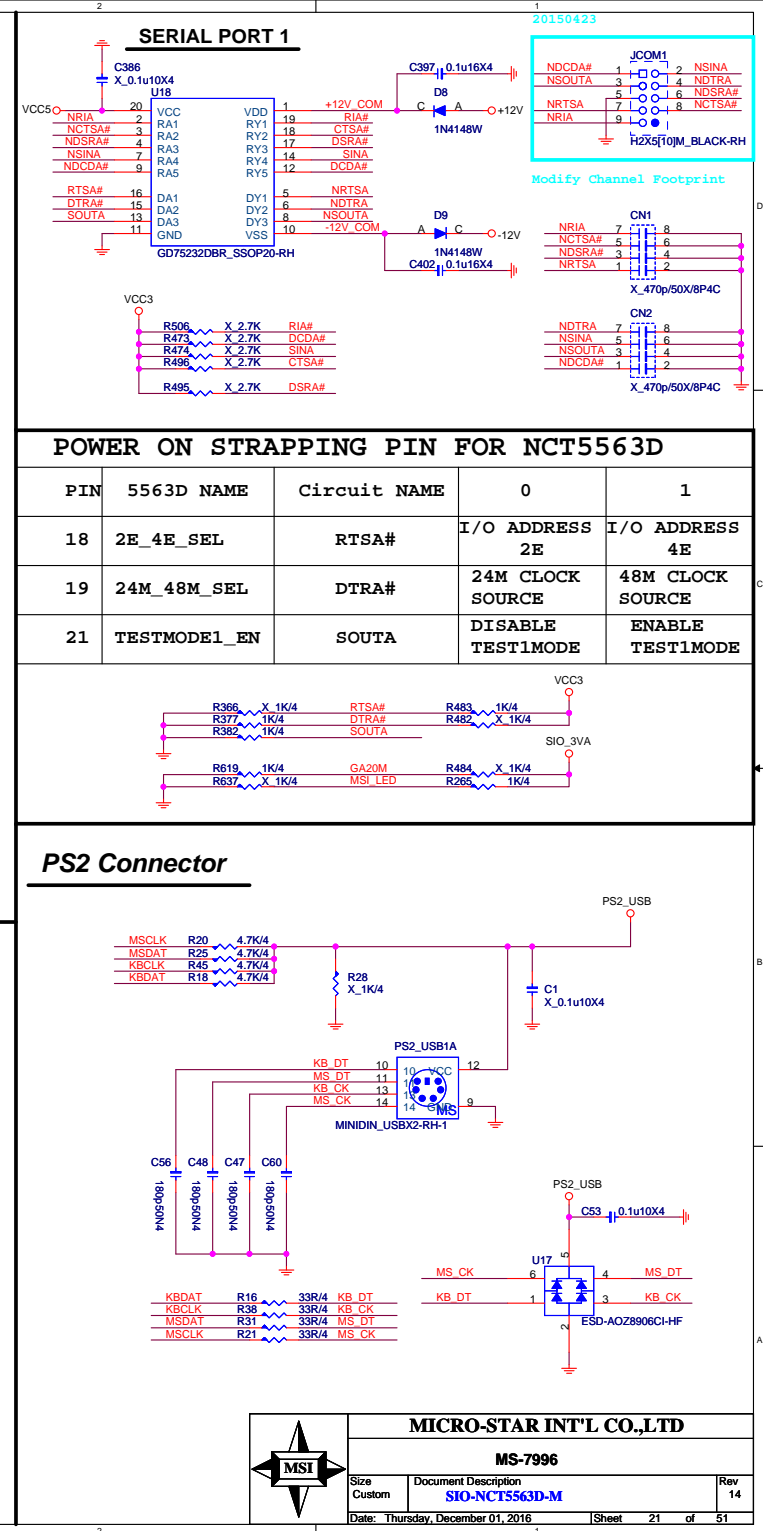
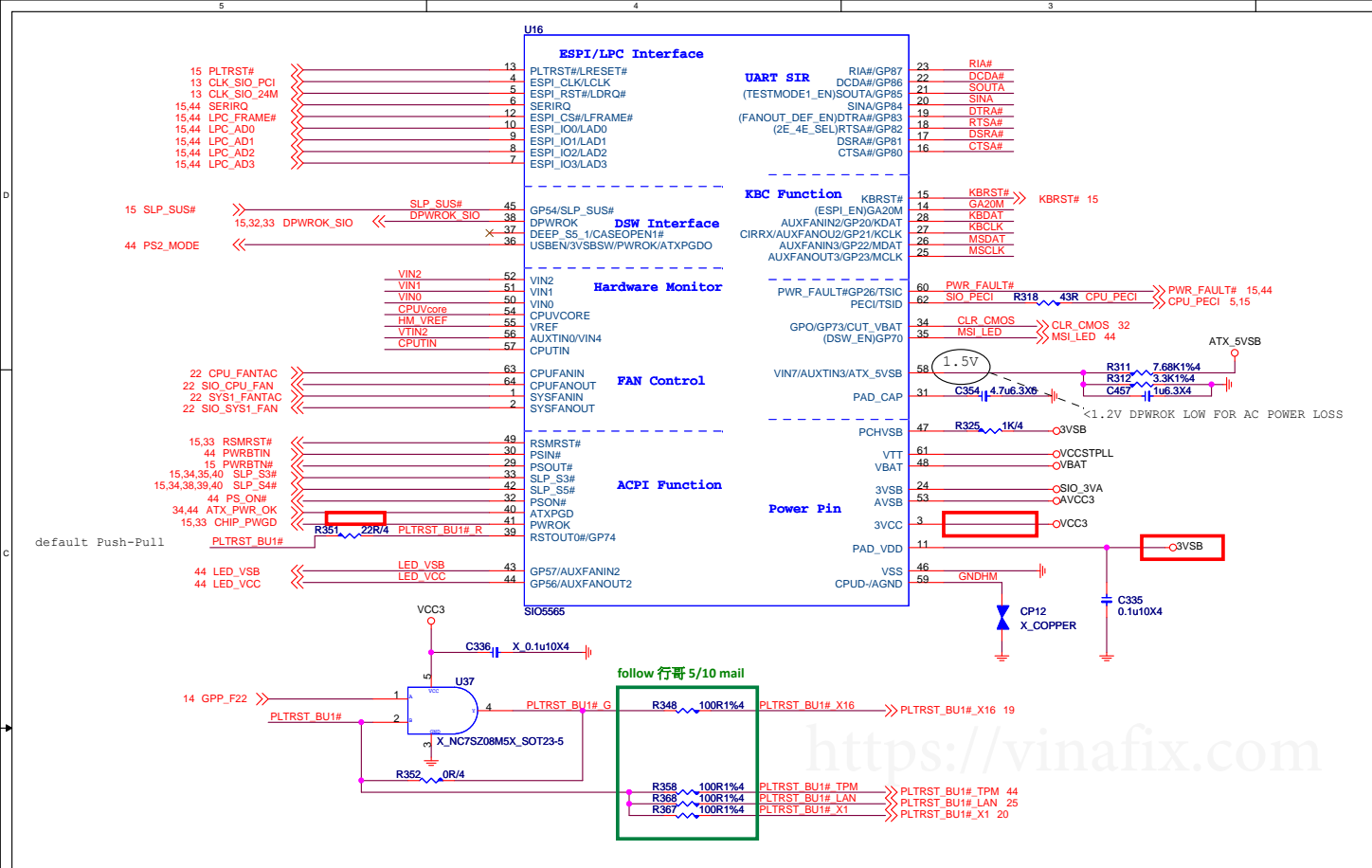
2015.6.16 add C75



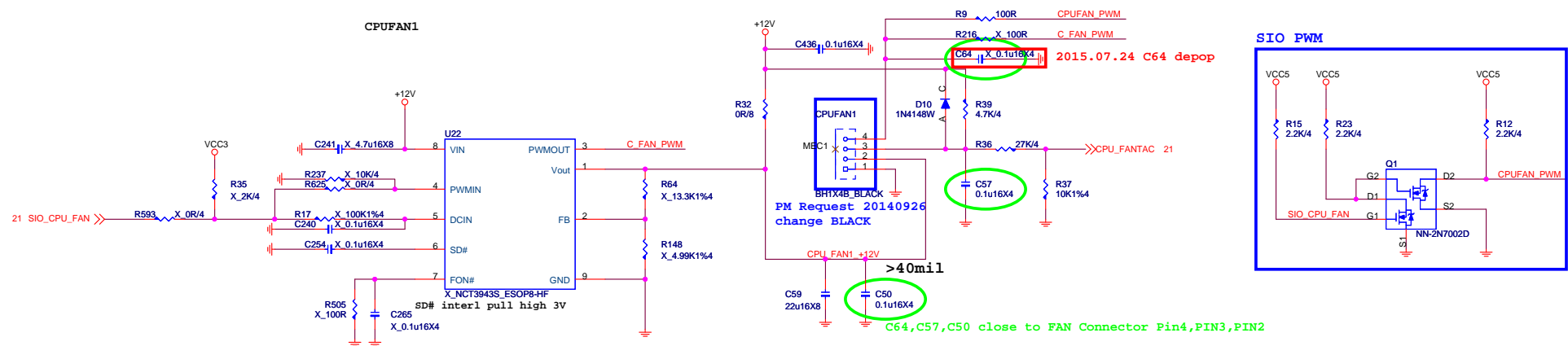
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		PCIE SLOT-PCH(X1)	14
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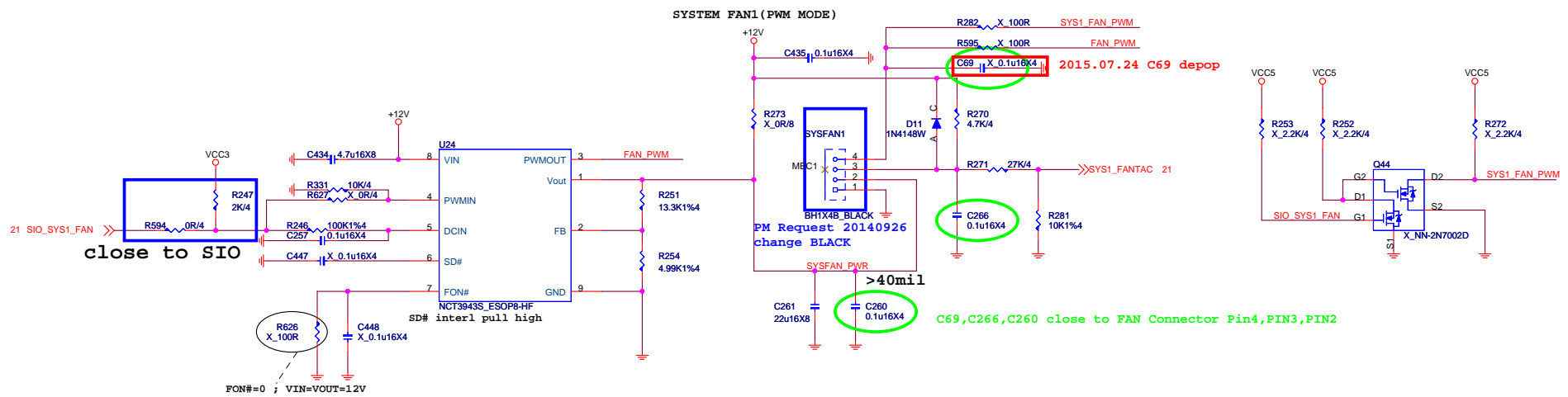


Type G : 4 PIN CPU FAN FROM SIO



CPUFAN_PWR_OFF
GPIO Control
Deafult GPI
If USE CUT POWER
1.OPEN DRAIN LOW:SD# LOW Active , CPUFAN(PIN2)= 0V
2.OPEN DRAIN : SD# Internal Pull high , CPUFAN(PIN2)=12V

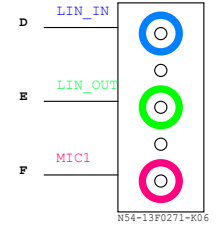
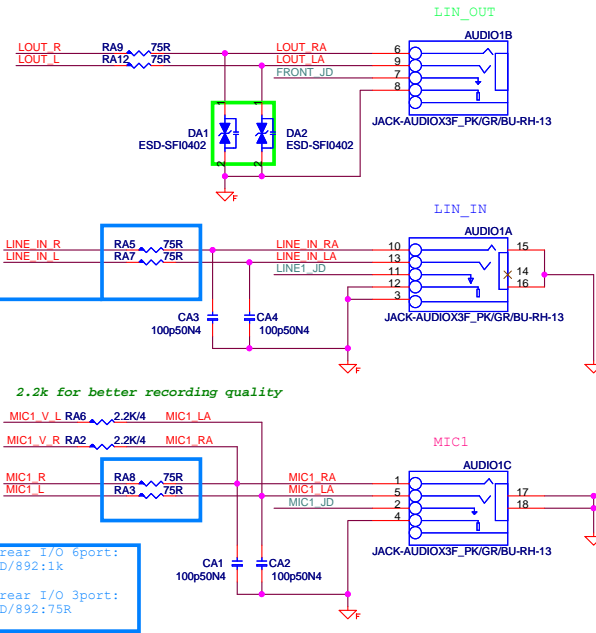
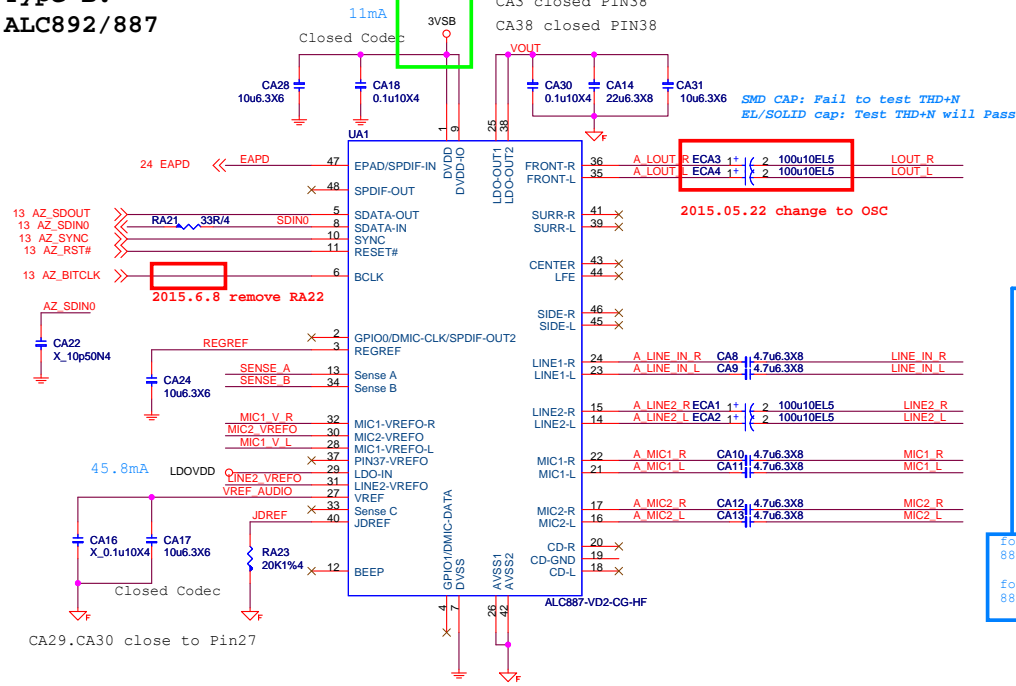
Type H : 4 PIN SYS FAN FROM SIO



Type B:
ALC892/887

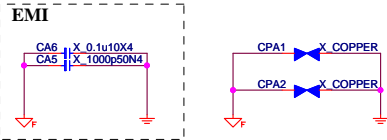
2014.09.15

CA4 closed PIN25
CA3 closed PIN38
CA38 closed PIN38

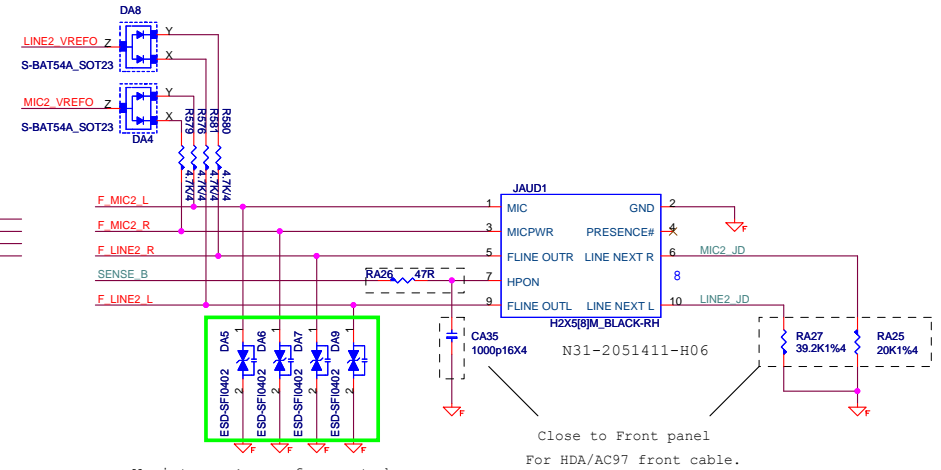
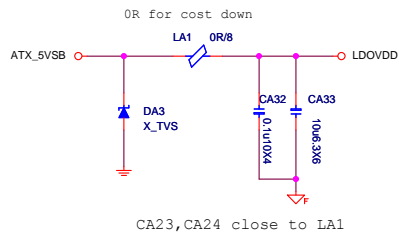


<https://www.vinafix.com>

Vinafix.com



Closed Codec



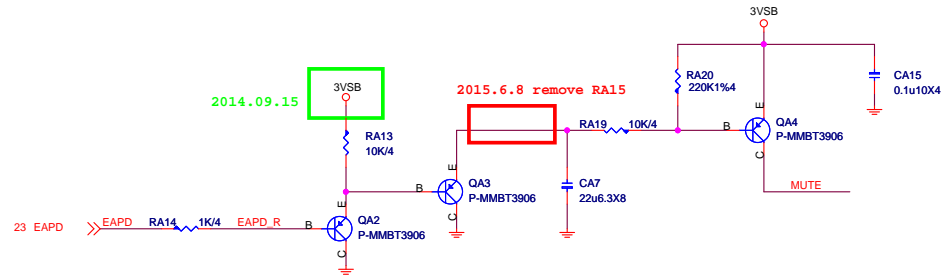
Varistor --> cap for cost down

D0G-2950500-SI0
D0G-3010510-I05
Close to Jack

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Custom	AUDIO - ALC892/887		14
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Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog



<https://vinafix.com>

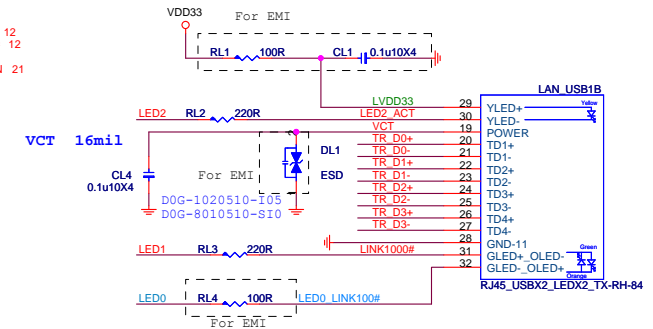
History:

2014/02/13: stuff de-pop circuit of Line out & HP out.

RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

LAN Connector



Pin33: 4 via from top layer to GND layer
and make the via at the center of IC.

<https://vinafix.com>

8111G POWER Consumption

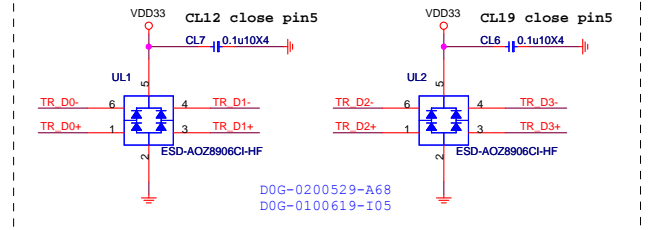
	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

ESD Protect

UL2&UL3 close to connector



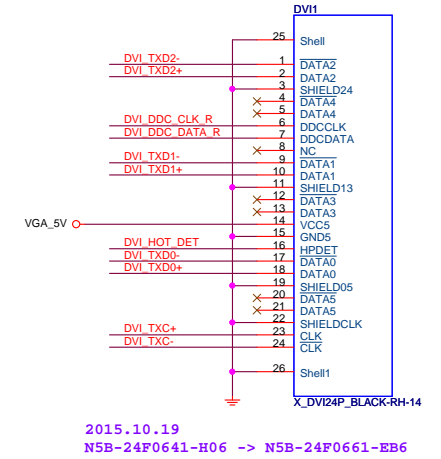
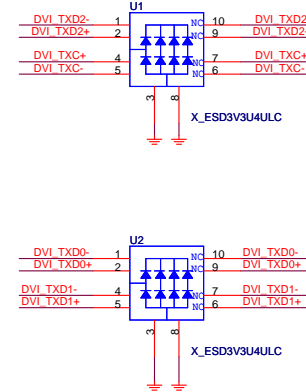
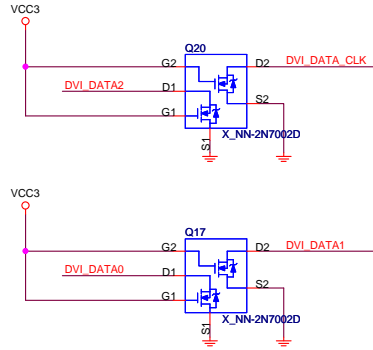
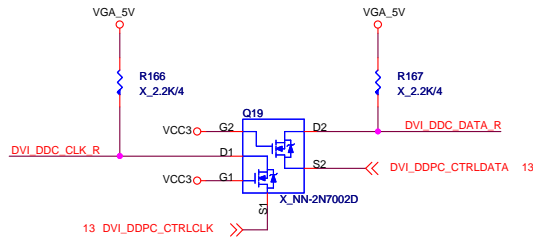
MICRO-STAR INT'L CO.,LTD

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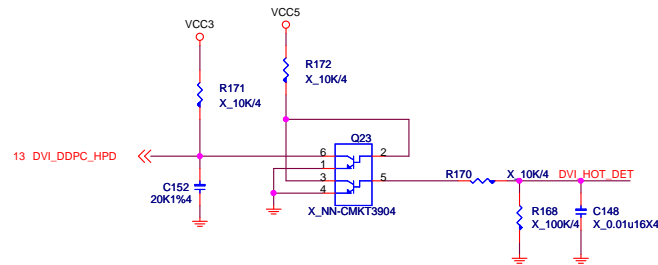
DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

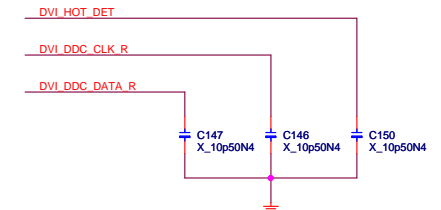
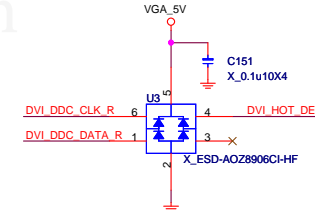
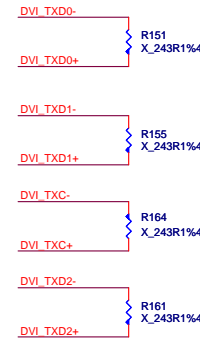


2015.10.19
N5B-24F0641-H06 -> N5B-24F0661-EB6

HPD

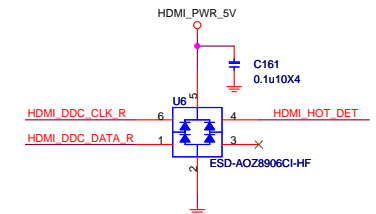
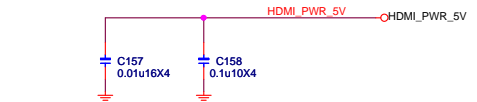
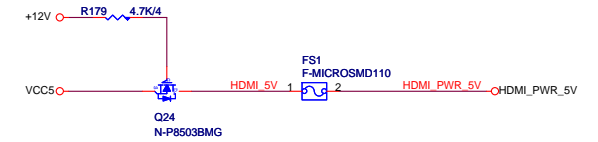
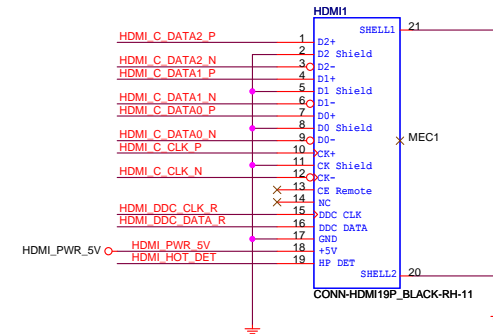
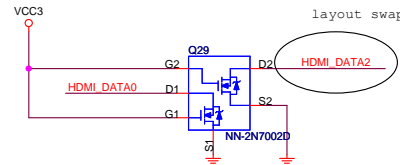
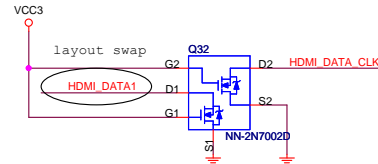
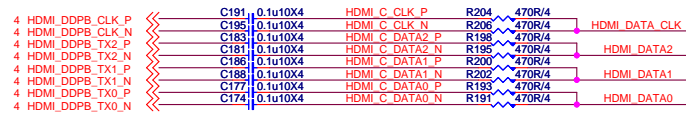


For EMI

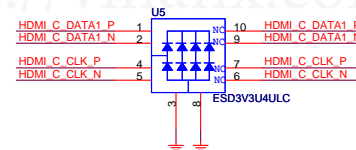
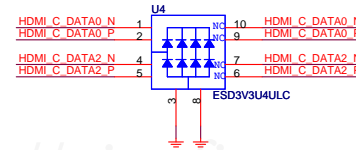
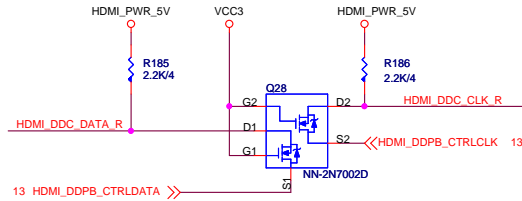


HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

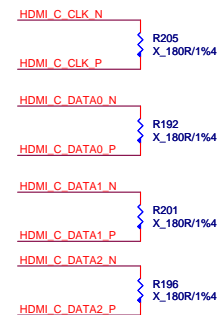
Vinafix.com



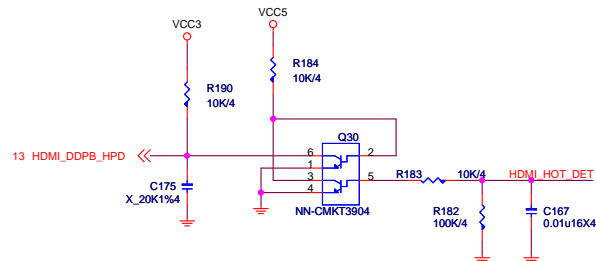
MICRO-STAR INT'L CO.,LTD			
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For EMI



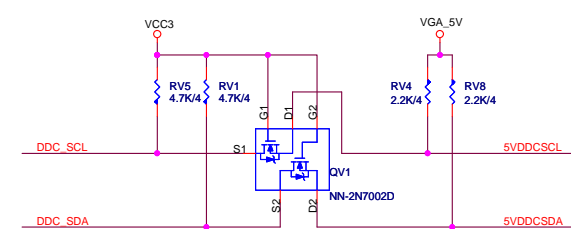
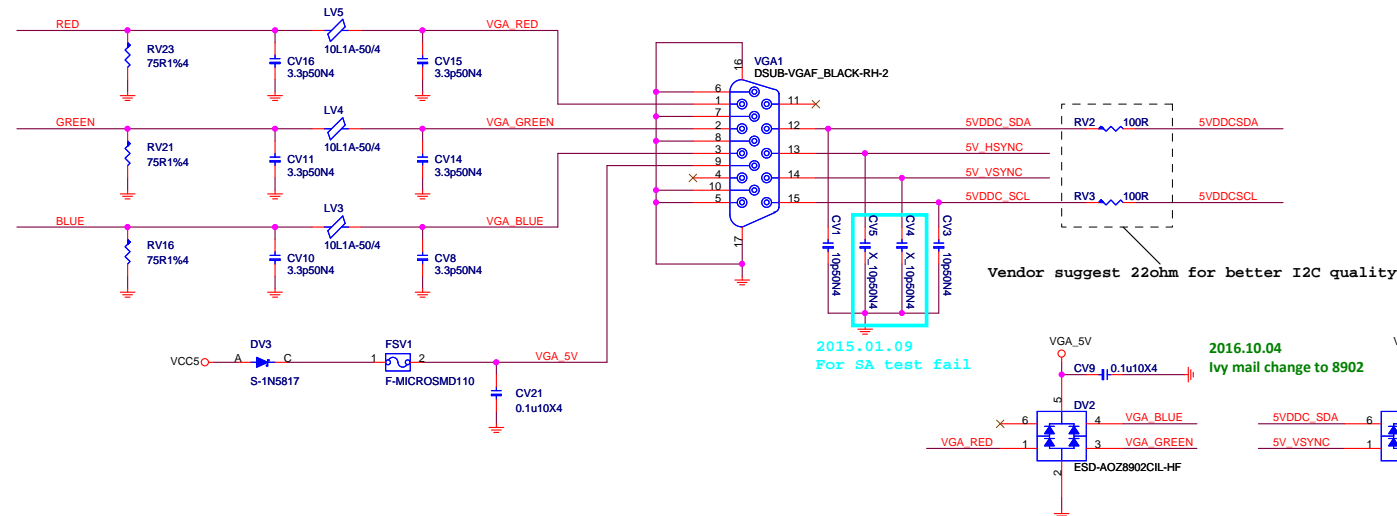
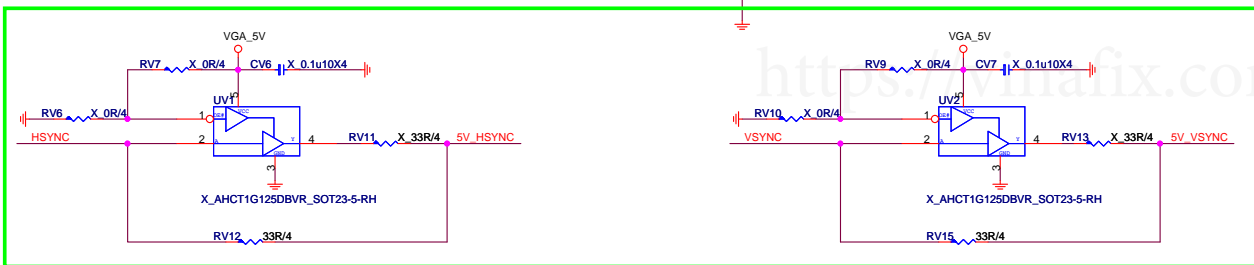
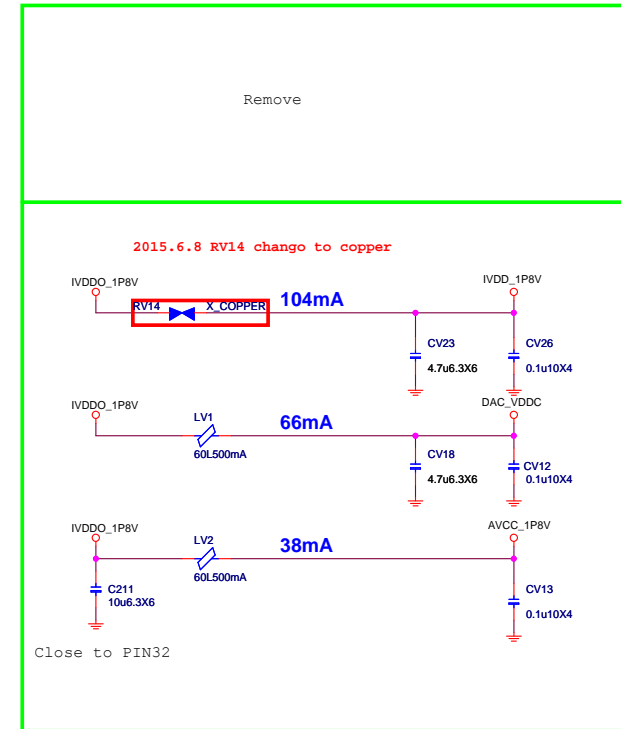
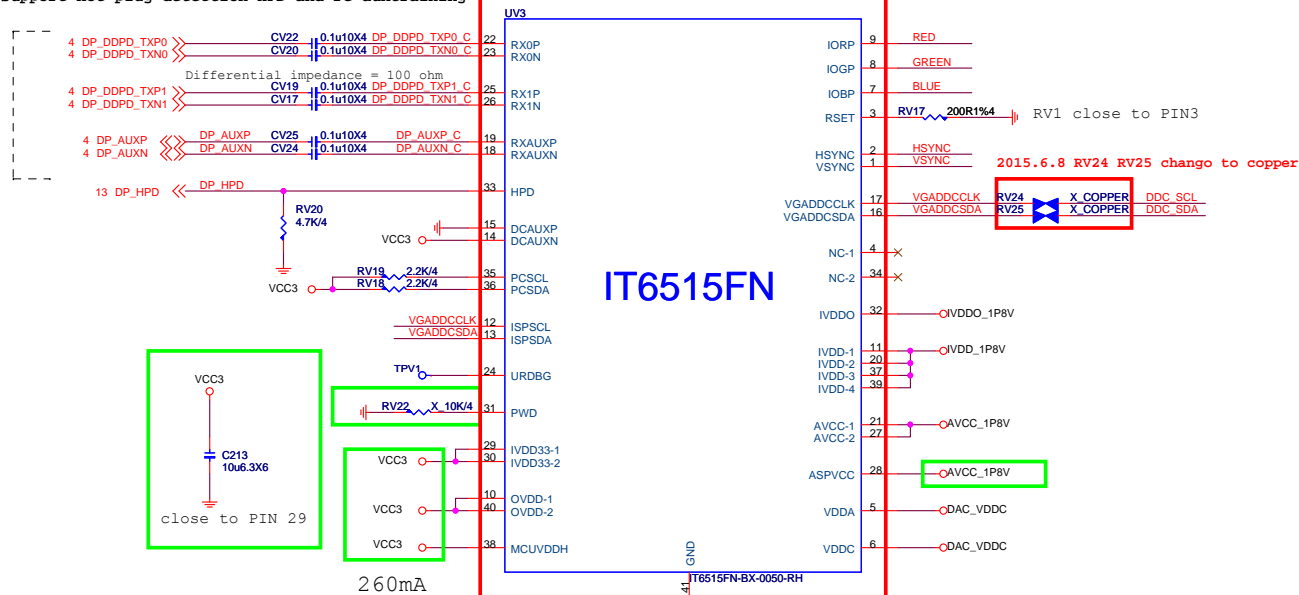
HPD

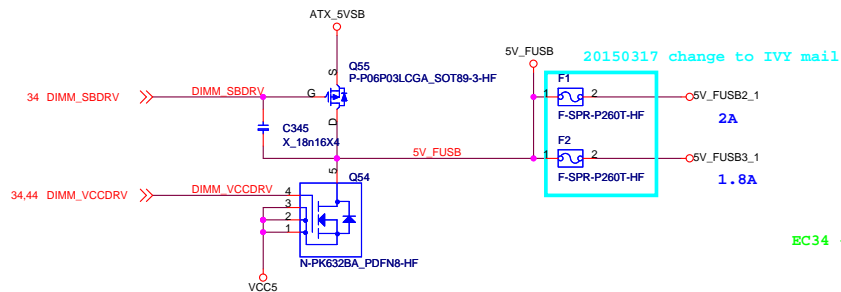


Note:

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

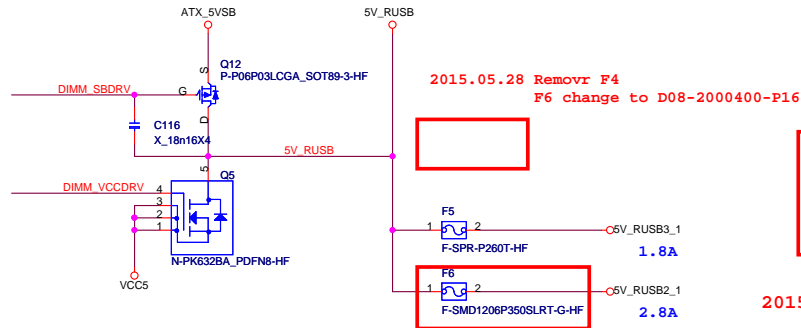
2015.05.22 UV3 change to B0B-6515F1C-II5



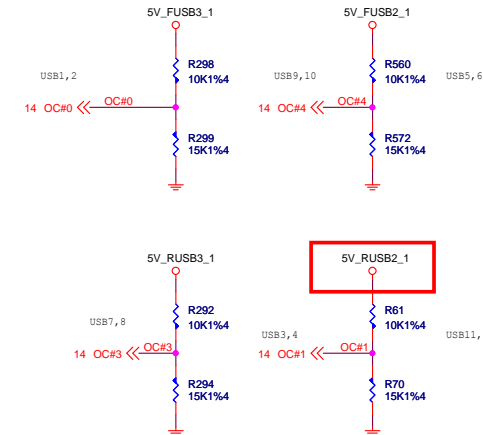


EC34 -> 560uF

2015.05.28 Remove USB CAP EC33

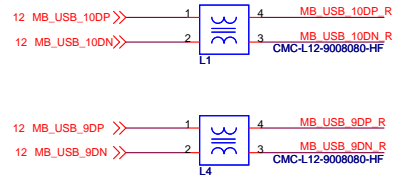


2015.05.28 Remove USB CAP EC3

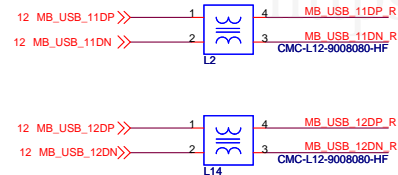


2015.05.28 change to 5V_RUSB2_1
2015.06.08 Remove R559, R575 and R605, R409

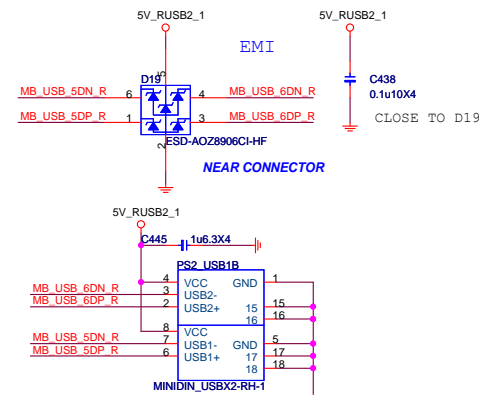
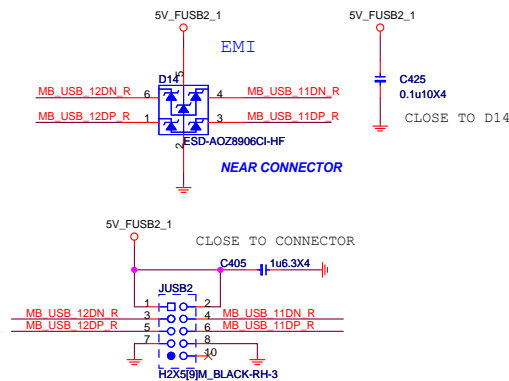
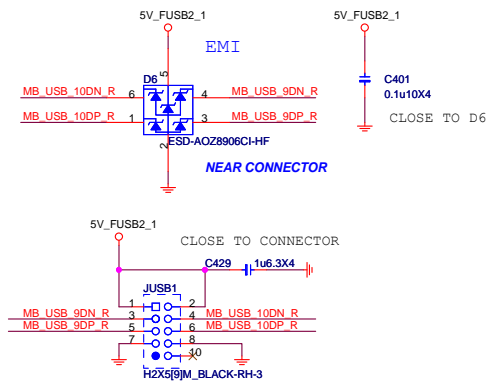
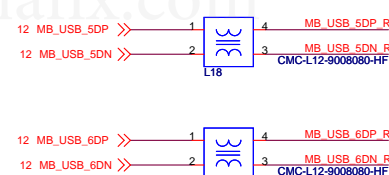
FRONT USB PORT 9,10



FRONT USB PORT 11,12

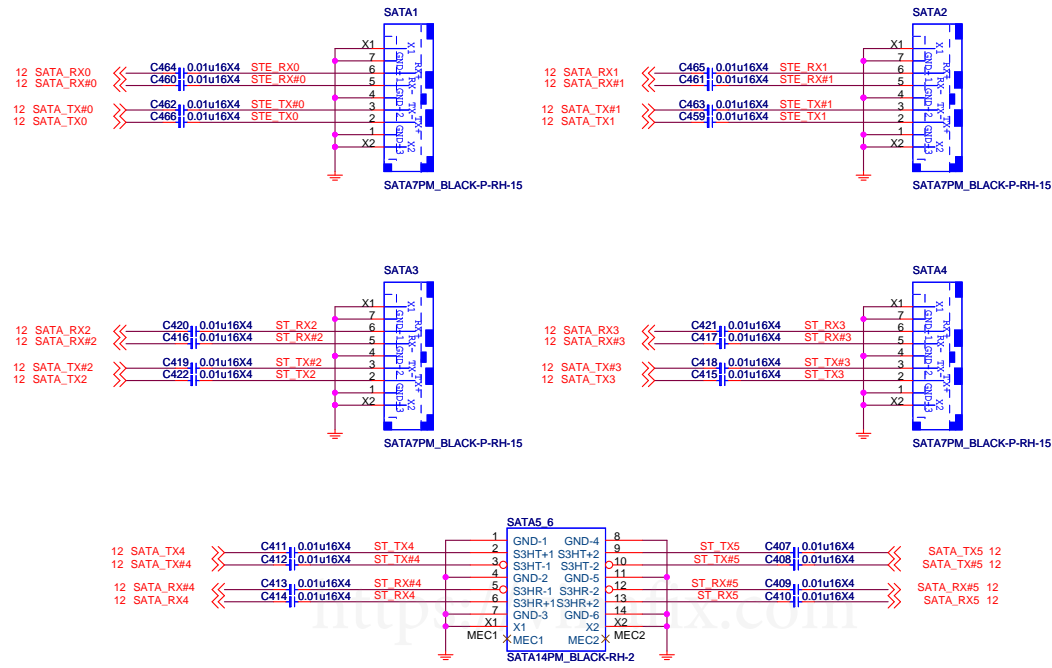


REAR USB PORT 5,6



2015.05.22 USB2 change to USB11,12
PS2_USB change to USB5,6

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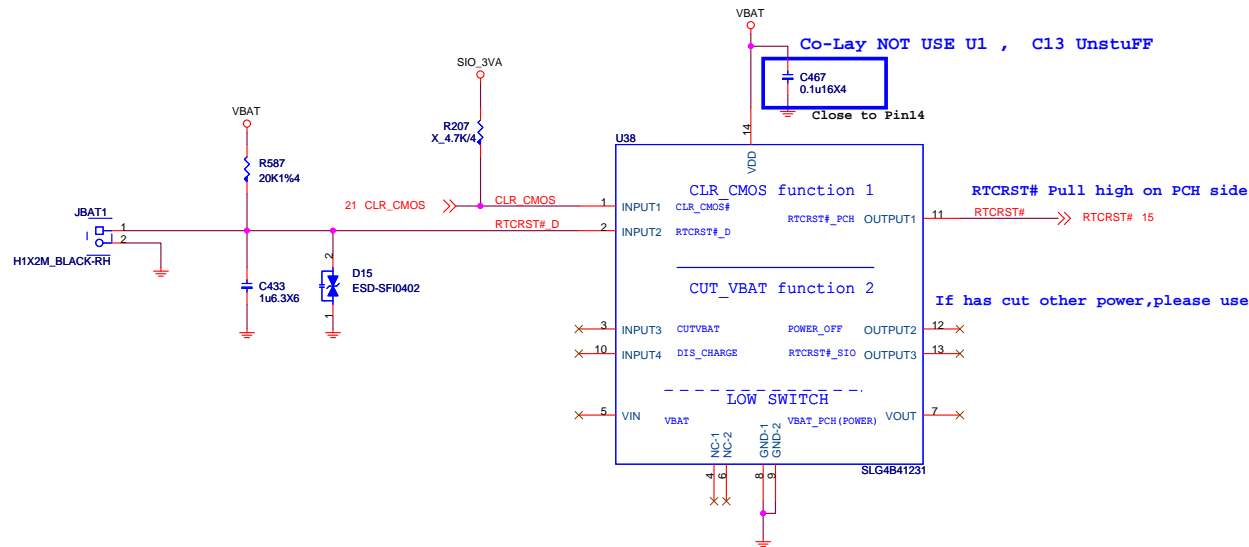


MICRO-STAR INT'L CO.,LTD

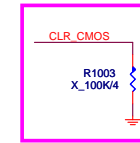
MS-7996

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CLR_CMOS



20160629



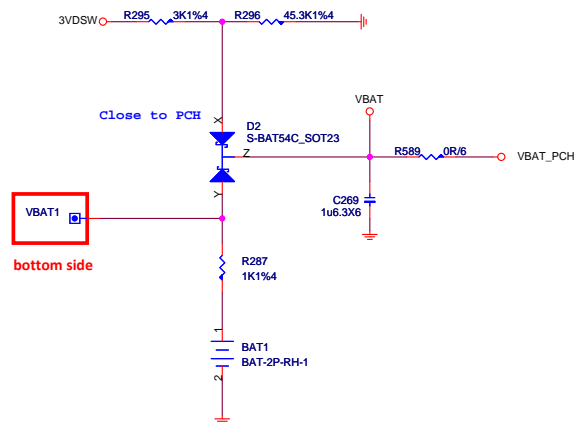
Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Vinafix.com

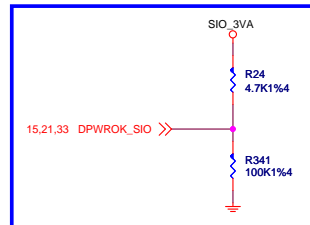
VBAT

<https://vinafix.com>

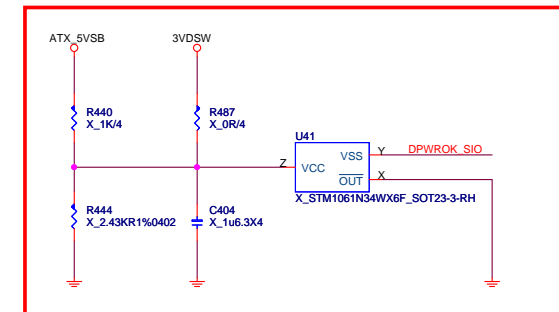


co-lay

RTCRST# R588 X_0R/4 RTCRST#_D 34



2015.6.10 add circuit



MICRO-STAR INT'L CO.,LTD

MS-7996

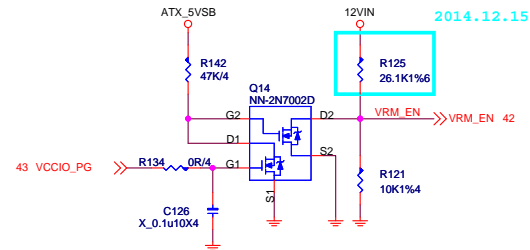
Size	Document Description	Rev
Custom	CUT_VBAT circuit	14
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A diagram showing a 3VSB power source connected to a circuit. The 3VSB source is connected to a 3VSR source, which is then connected to a circuit. The circuit includes a 3VSB source, a 3VSR source, and a 3VSB source.

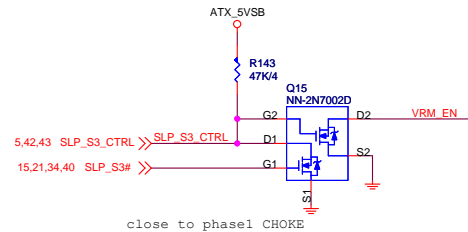


D03-0341409-A68 / D03-0230019-A30

Vinafix.com

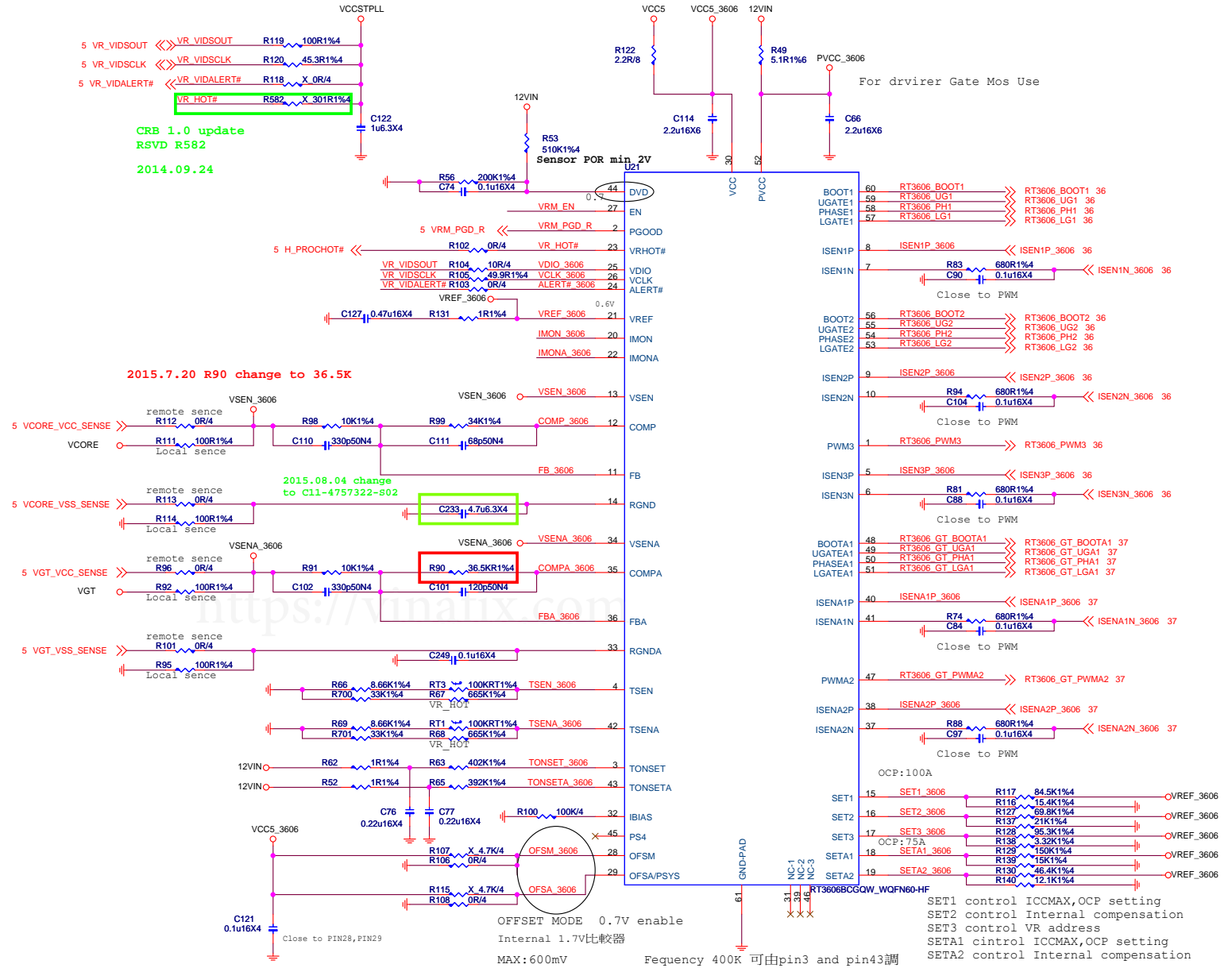


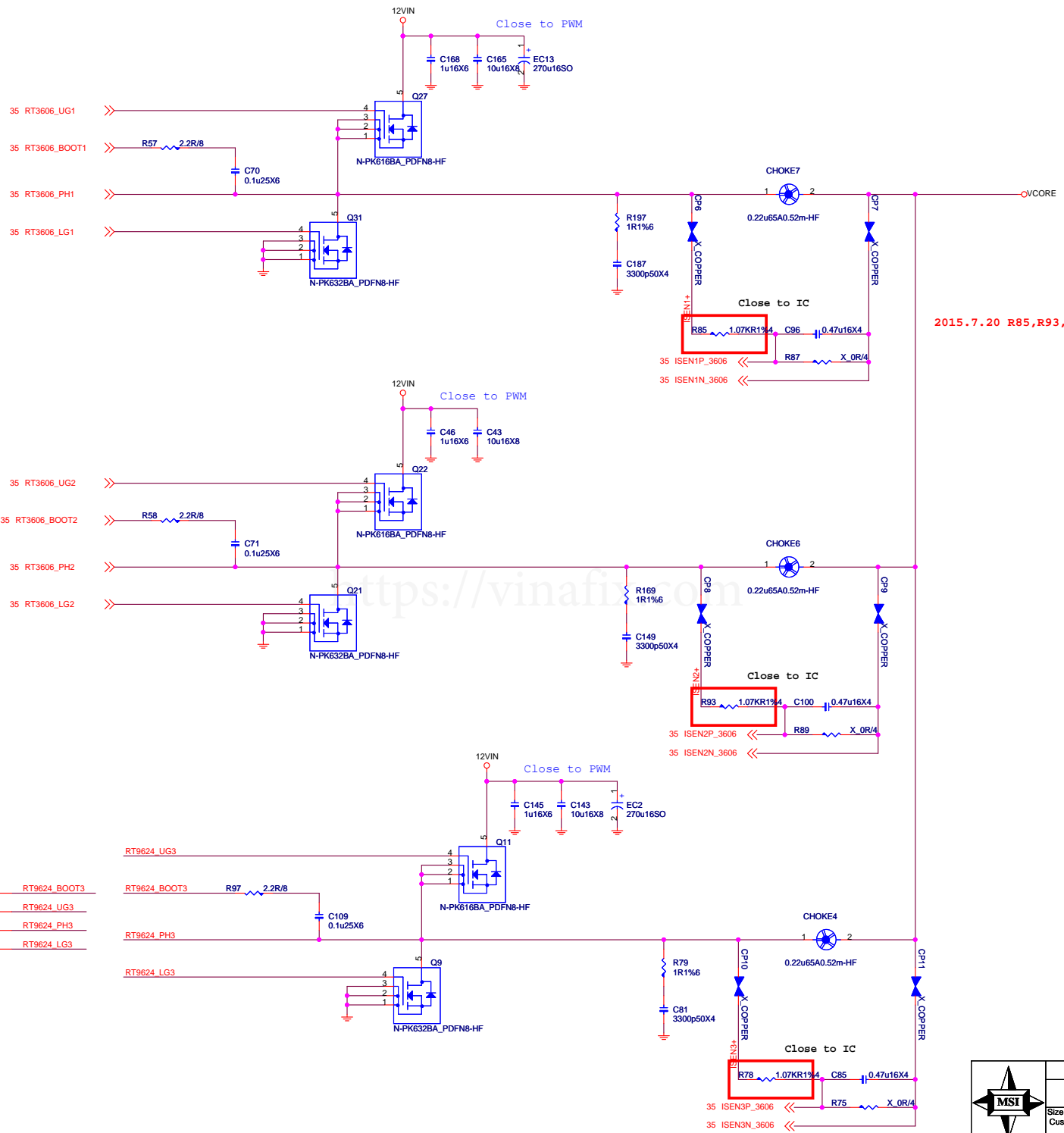
SLP_S3# assertion to IMVP VRM_EN deassertion
max:ilus



2015.7.20 R144 change to 13.7K

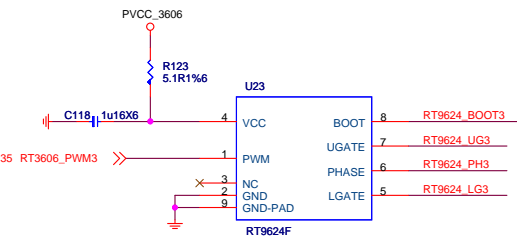
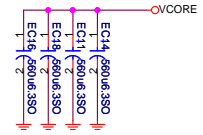
2015.7.20 R132 change to 23.7K






ICCMAX: 79A
LL: 2.1m ohm

2015.7.20 R85,R93,R78 change to 1.07K

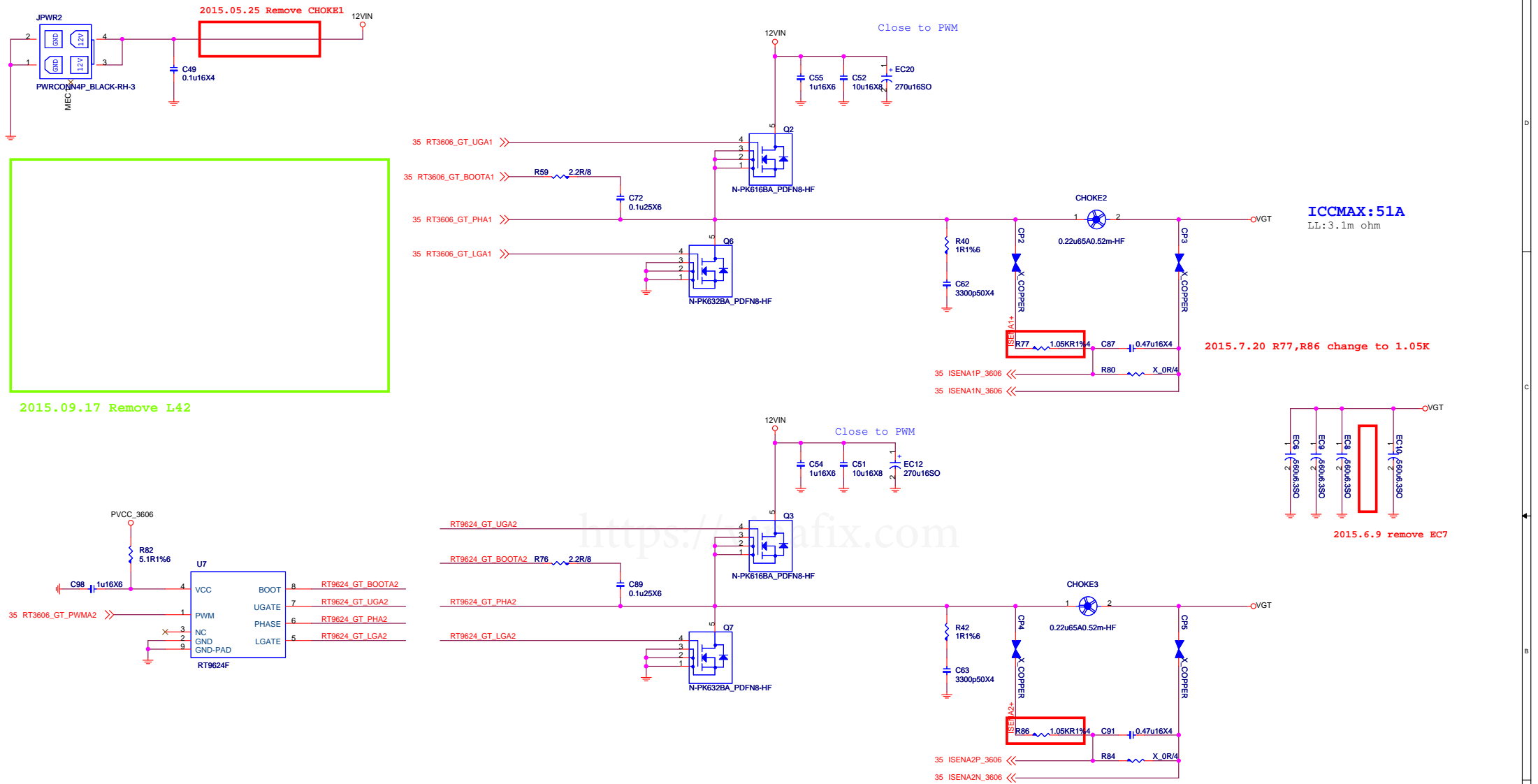




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ICCMAX:51A
LL:3.1m ohm

2015.7.20 R77,R86 change to 1.05K

2015.6.9 remove EC7



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DDR4_1.2V 2.8A+ 4.75A+0.375A=7.925

2.8A FOR CPU
4.8A FOR 2DIMM DDR4
0.375A FOR VTT_DDR

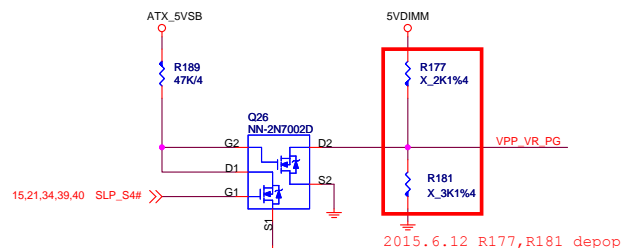
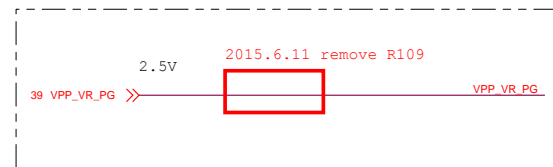
OCP = 7.925A*1.5=11.8875A

Current limit= 95.3K(R1054)*5uA/10/4mohm)=11.91A

2015.05.22 change to DDR4

VID	Reference Voltage (V)
H	0.675
L	0.75

$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))} \\ &= 9.357 * 0.44 \\ &= 4.154A \end{aligned}$$

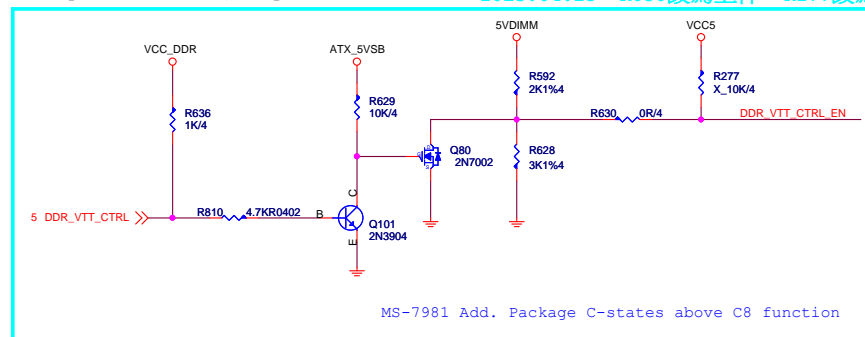


2015.6.11 remove circuit



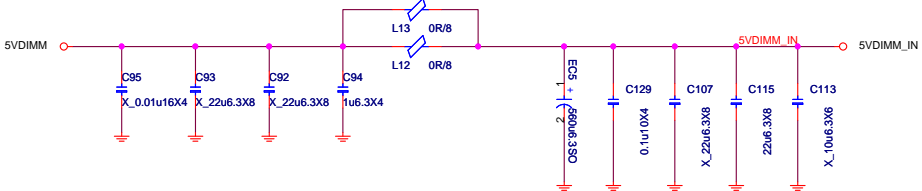
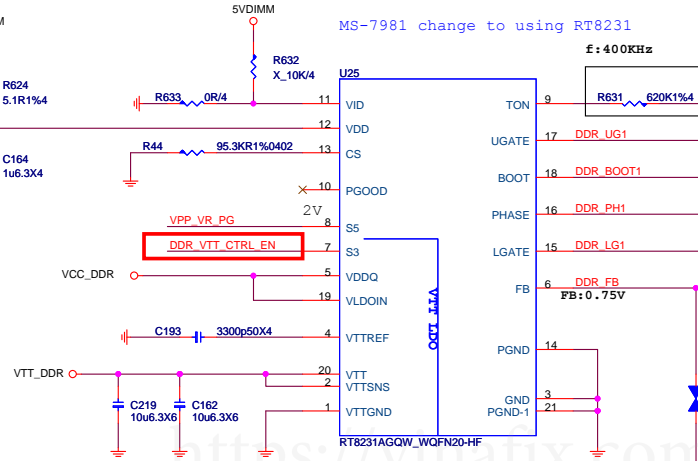
SLP_S4# de-assertion to VDDQ ramp down start

VPP ramp down after VDDQ ramp down



MS-7981 Add. Package C-states above C8 function

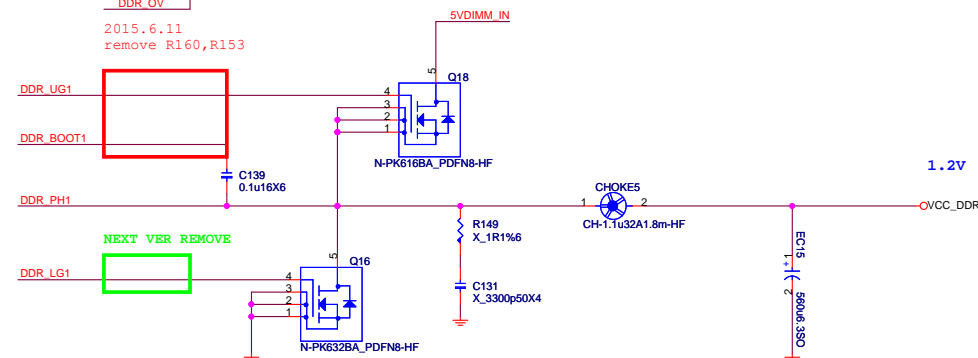
MS-7981 change to using RT8231



By layout modify

MAX: 7.925A

1.2V

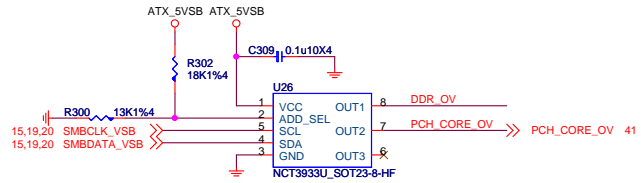


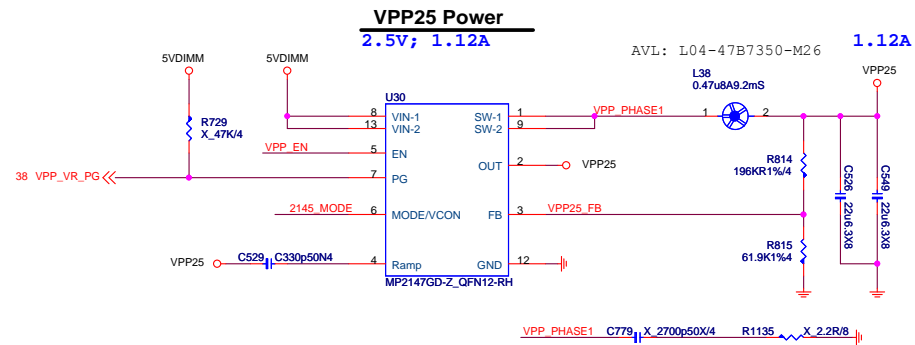
2015.6.11 remove R160,R153

NEXT VER REMOVE

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K





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PCH 1VSB

1.0V; 7.858A

OCp = 11.787A

Rocset = $1.5 * I_{max} * R_{dson}(low) / I_{ocset}$
 = $1.5 * 7.858 * 5mohm / 10uA$
 = 5.8935K

Rocs: 5.9K, OCp:

D03-4C05N03-005 : 11.8A

D03-632BA0C-N03 : 12.82A

use UBIQ MOS need Check

Rdson(low) 4.5V

D03-4C05N03-005 : 5 mohm

D03-632BA0C-N03 : 4.6mohm

D03-3056M00-U47 : 6.2mohm

2015.04.23 change to UP1540

2014.08.22 close to U34

2015.01.22
 for up1540:stuff R438->36K,
 C379->NC, C373->3.3nF
 for RT8125:R438.C379.C373->NC

2015.01.22
 for up1540:R403->2.2R, C362->1uF
 for RT8125:R403->10R, C362->1uF

$$I_{rms} = I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

MAX:10.664A

$$I_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

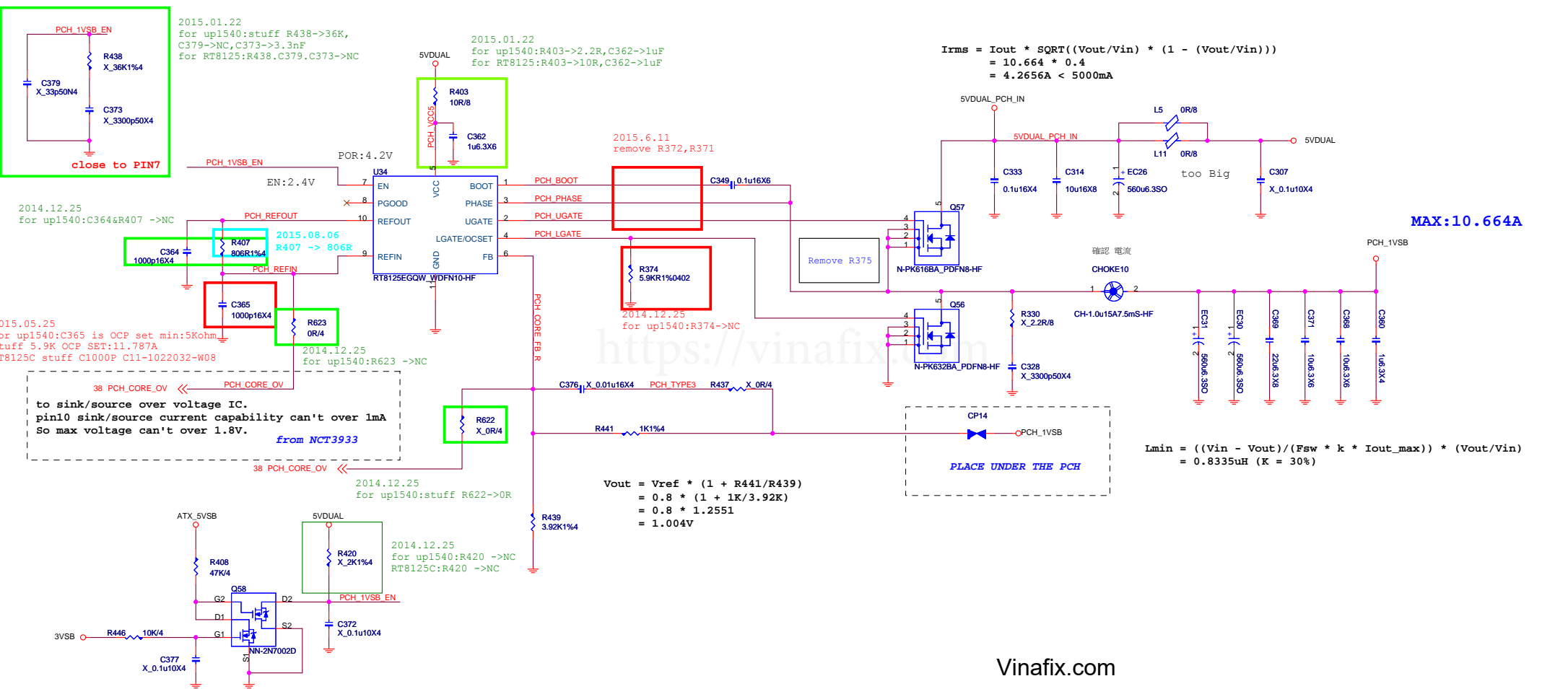
$$= 0.8335uH (K = 30\%)$$

$$V_{out} = V_{ref} * (1 + R_{441}/R_{439})$$

$$= 0.8 * (1 + 1K/3.92K)$$

$$= 0.8 * 1.2551$$

$$= 1.004V$$



Vinafix.com

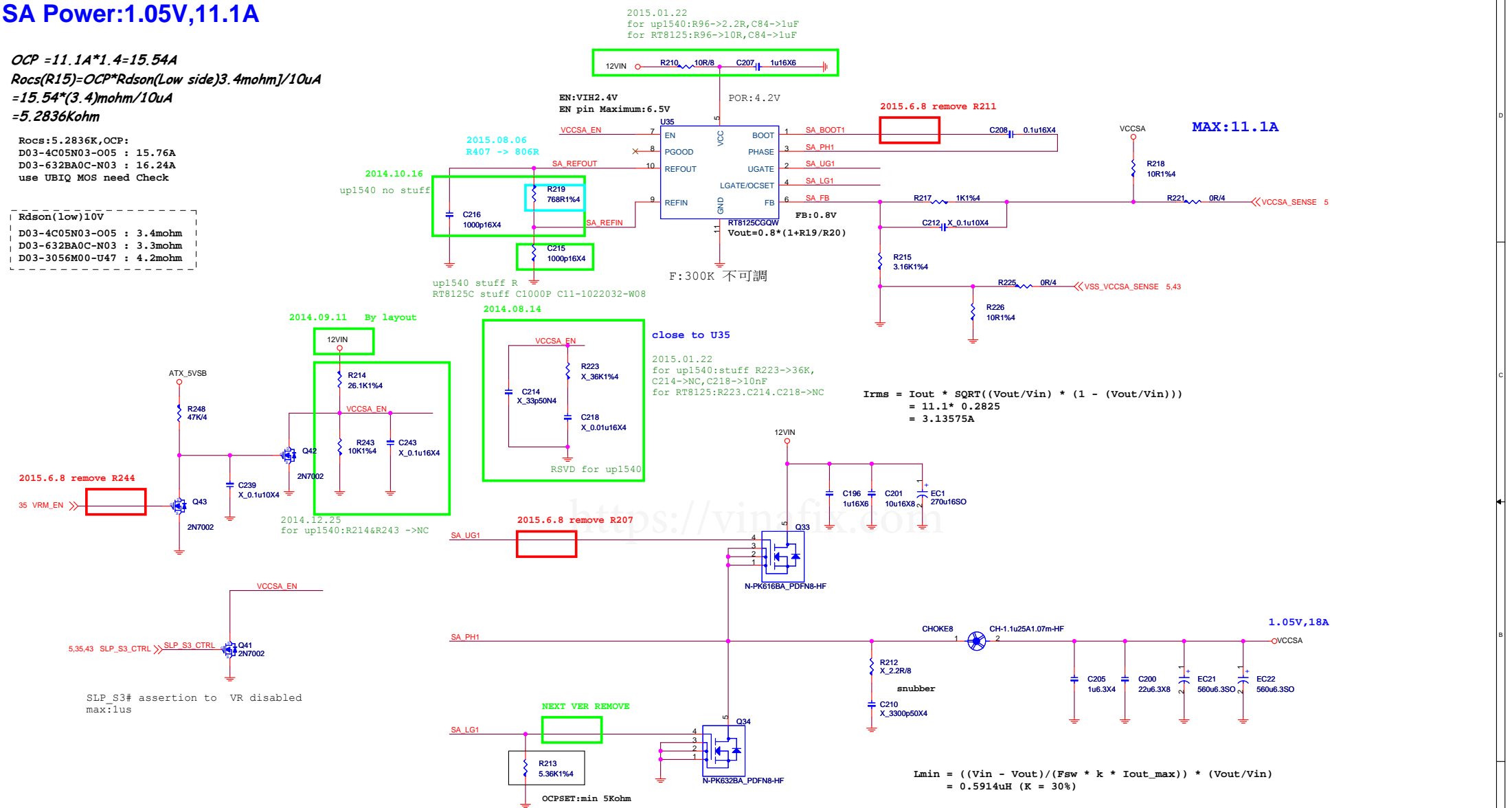
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SA Power:1.05V,11.1A

$OCP = 11.1A * 1.4 = 15.54A$
 $R_{ocs}(R15) = OCP * R_{dson}(Low\ side) / I_{outA}$
 $= 15.54 * (3.4)mohm / 10uA$
 $= 5.2836Kohm$

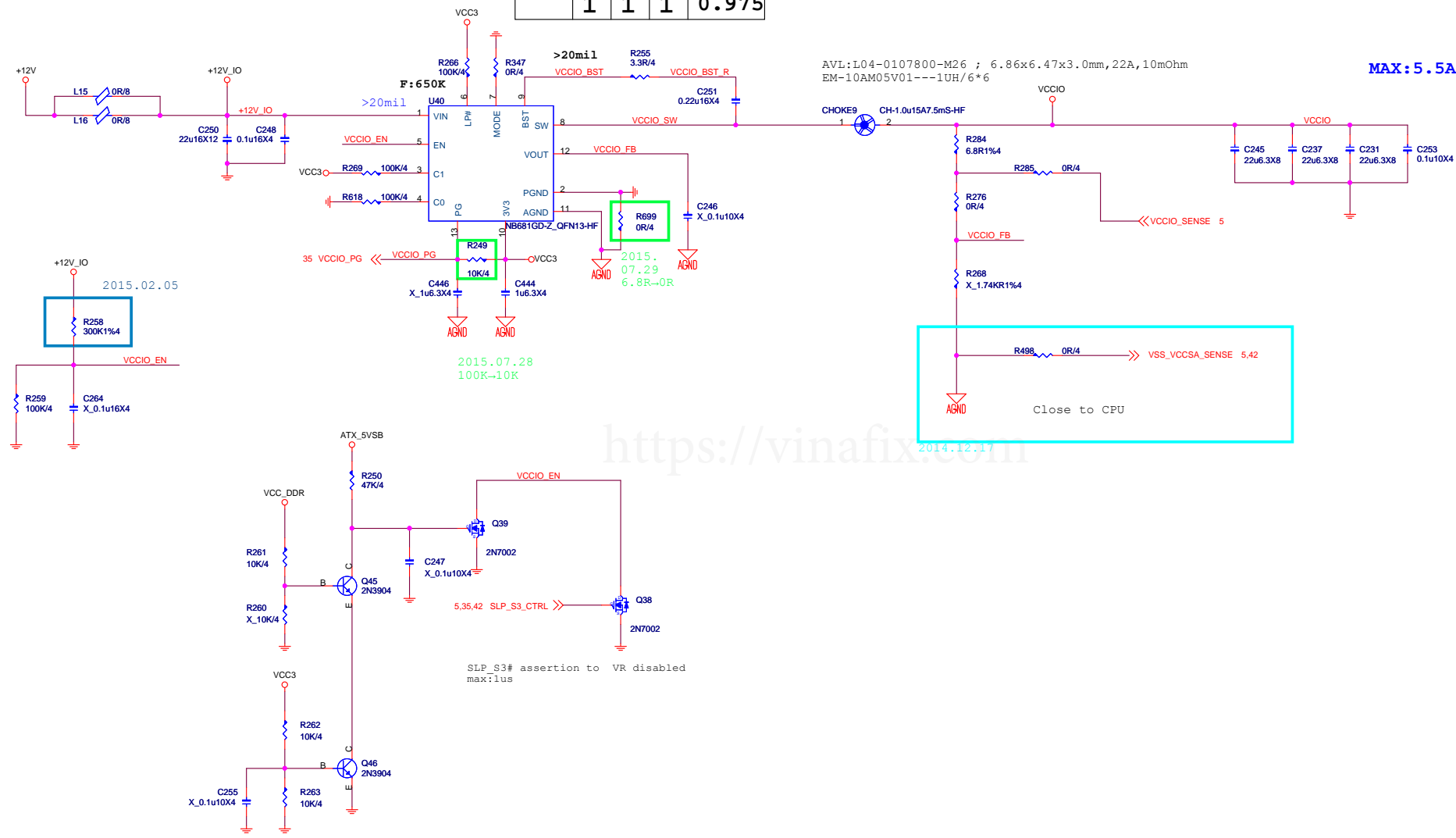
- Rocs:5.2836K,OCP:
D03-4C05N03-005 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check
- Rdson(10V)10V

D03-4C05N03-005 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

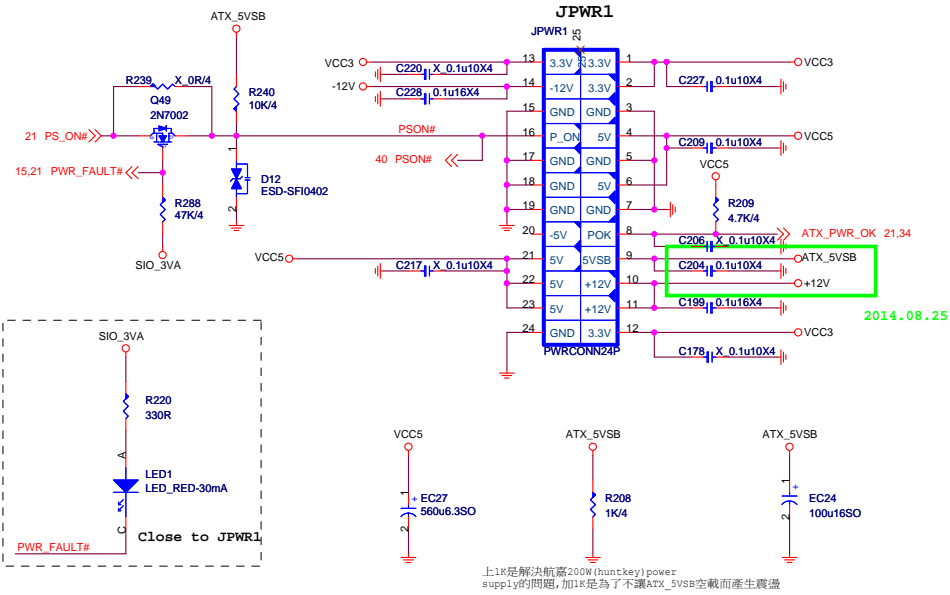


VCCIO
0.95V; 5.5A
IMAX 6A
ILIMIT=8.5~9A

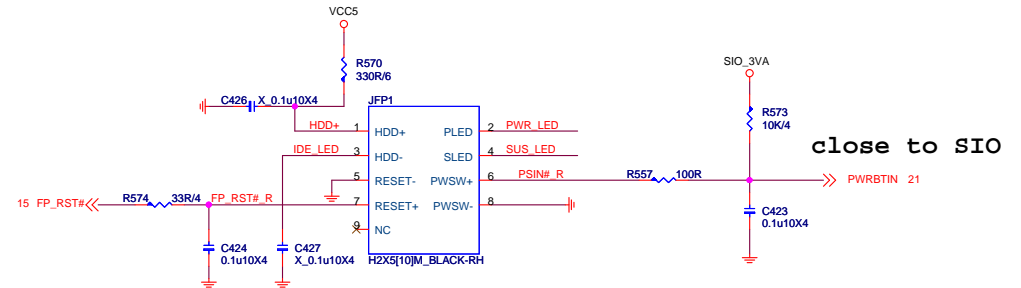
	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975



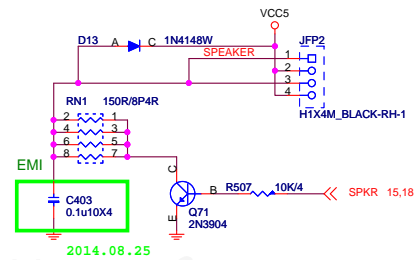
ATX POWER CONNECTOR



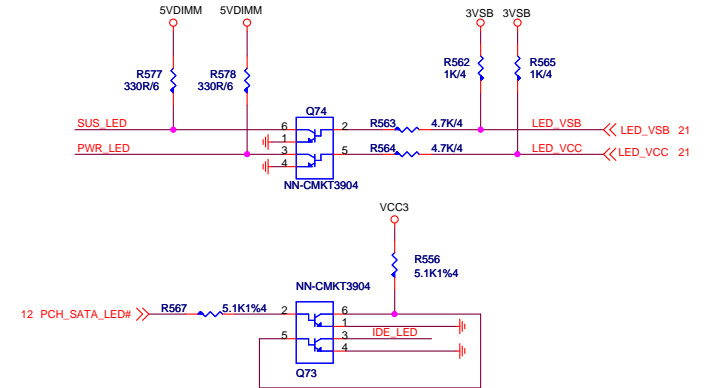
FRONT PANNEL



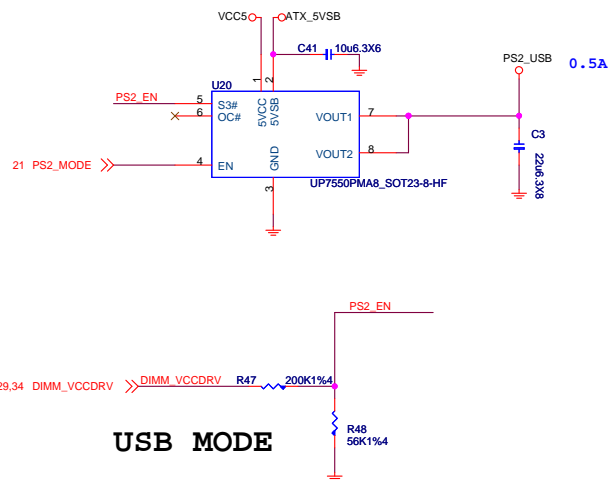
Speaker Pin Header



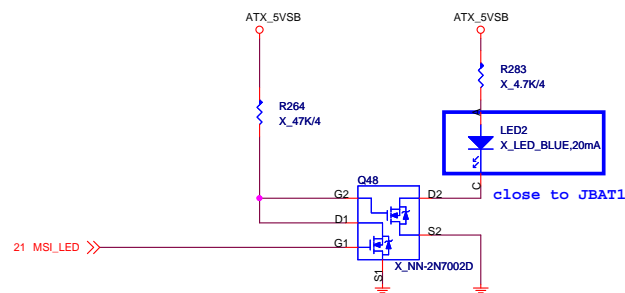
LED (for NV5533)



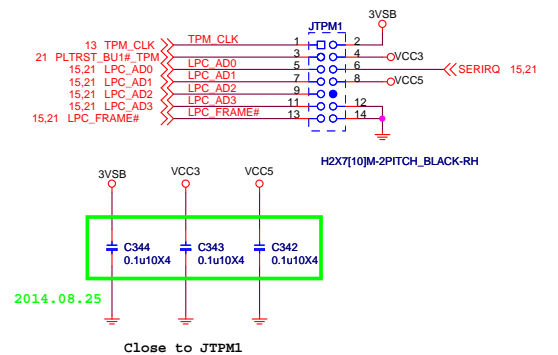
PS2 POWER



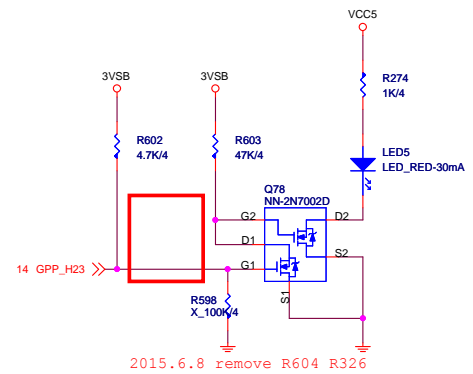
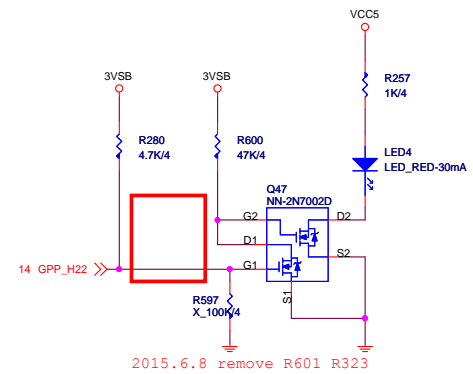
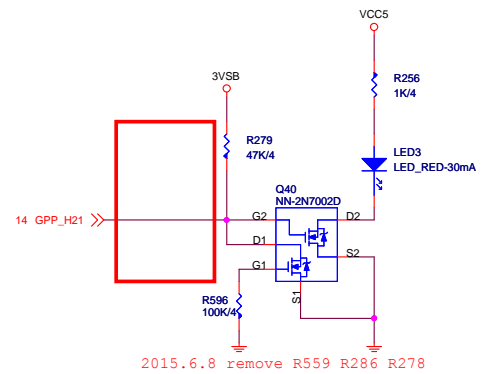
MSI LED



TPM



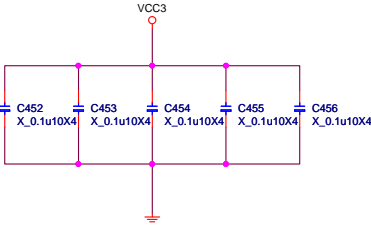
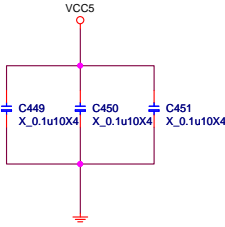
DEBUG LED



GPIO LED	GPP_H21	GPP_H21	GPP_H21
	GPI PULL HIGH	GPO PO LOW	GPO PO LOW
亮			
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

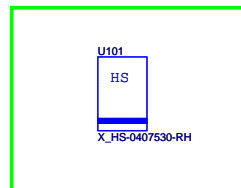
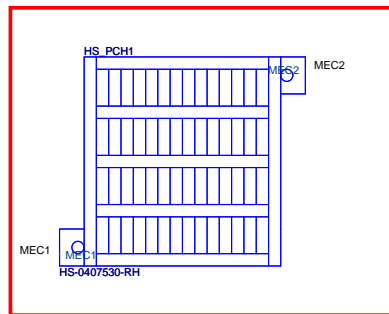
- 關機斷電狀態下，3個LED先維持default全暗，開機通電後：
1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
 2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
 3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
 4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

EMI CAP

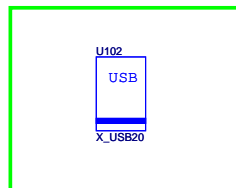


<https://vinafix.com>

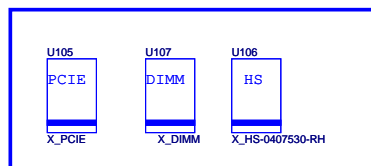
2015.06.01 change to using E31-0407530-K08



2015.08.03
colay Heatsink for H110

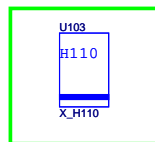


2015.08.03
USB2.0 Connector colay for H110

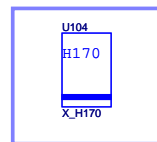


2016.05.04 change PCIE slot + DIMM + HS
for B150M G1 GAMER

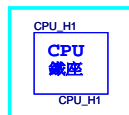
2015.08.03
PCH H110 colay



2015.08.10
PCH H110 colay



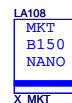
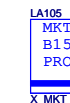
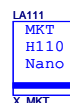
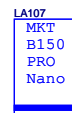
20150423 PM Request cost down



客戶LOGO貼紙

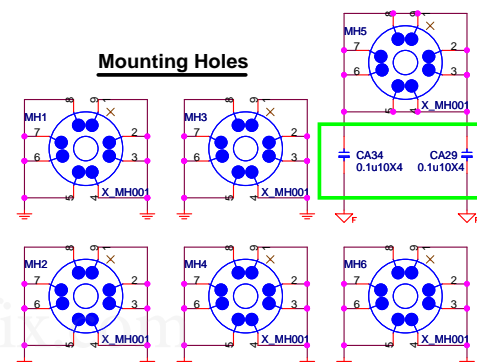


Marketing Name貼紙



2016/11/25 PK0-0799614-E48, 競華, 15, 寶安恩斯邁廠 (MSIS)
2016/11/25 PK0-0799614-G37, 精成-深圳, 15, 寶安恩斯邁廠 (MSIS)

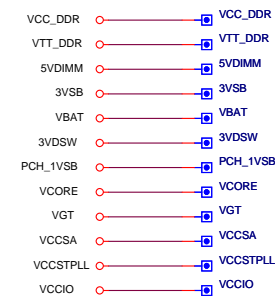
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Optical Fiducial Marks-120



Simulation



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